

# ZQA SOLE UMA SYSTEM DIAGRAM

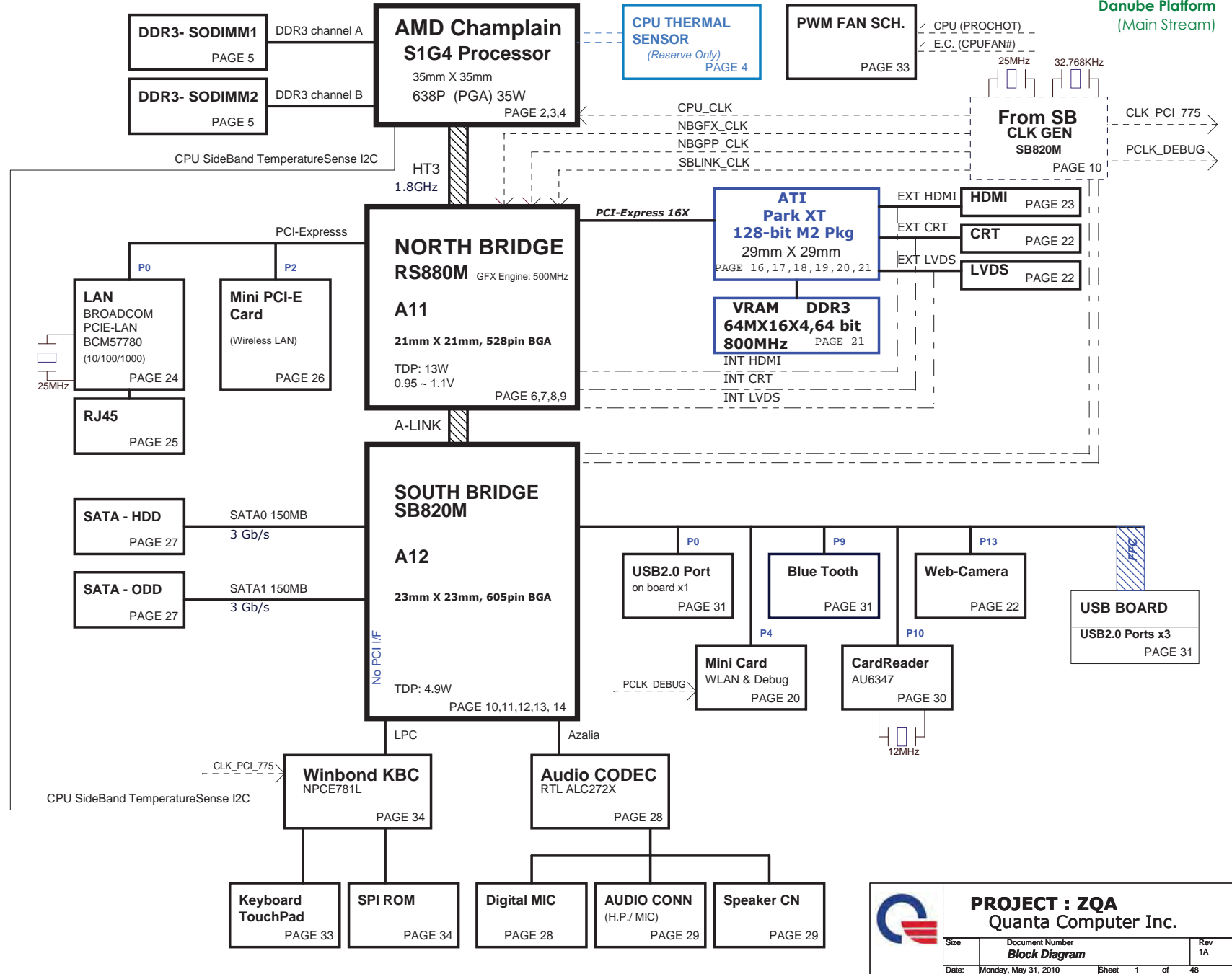


Danube Platform  
(Main Stream)

**PCB STACK UP**

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

IV@ -----> iGPU EV@ -----> dGPU  
SPE@ -----> Option Notice

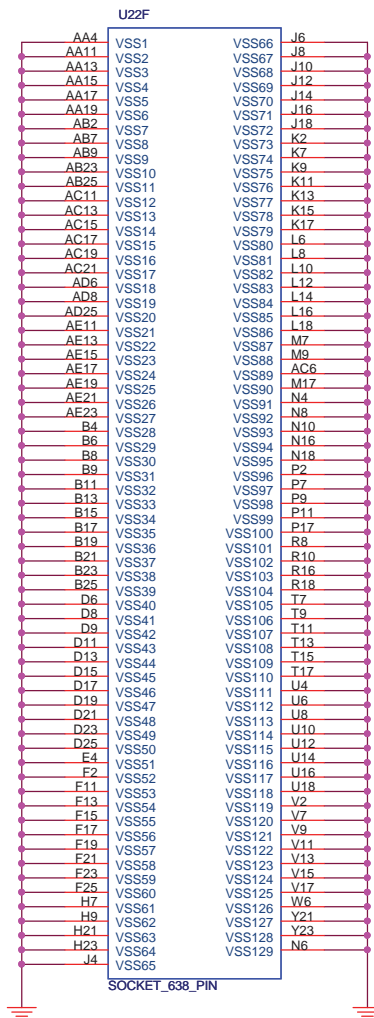
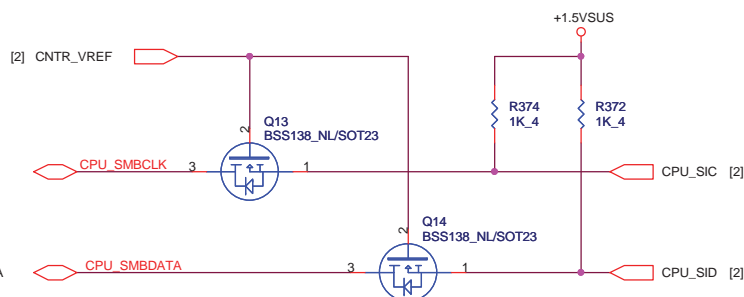
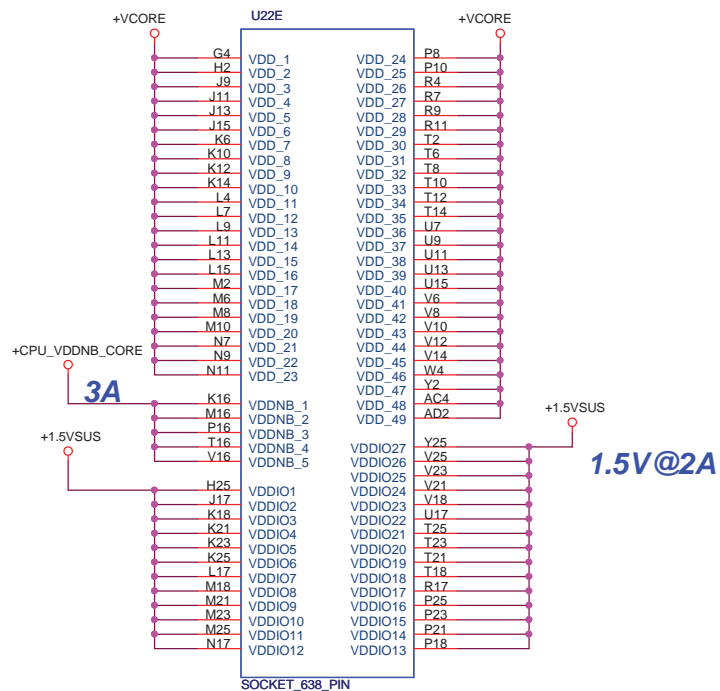


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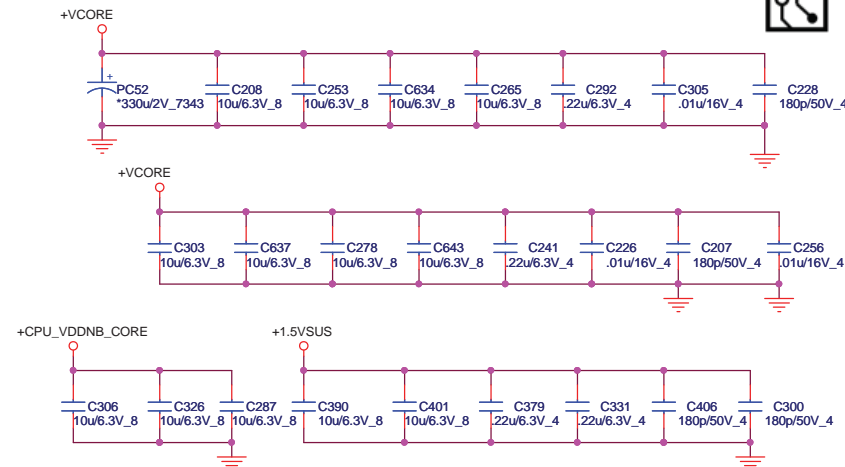
Size	Document Number	Rev
	<b>Block Diagram</b>	1A
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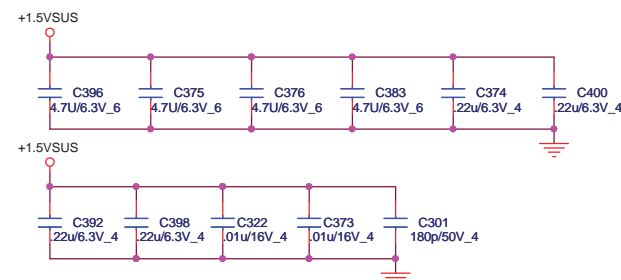


## BOTTOM SIDE DECOUPLING



## DECOUPLING BETWEEN PROCESSOR AND DIMMs

PLACE CLOSE TO PROCESSOR AS POSSIBLE

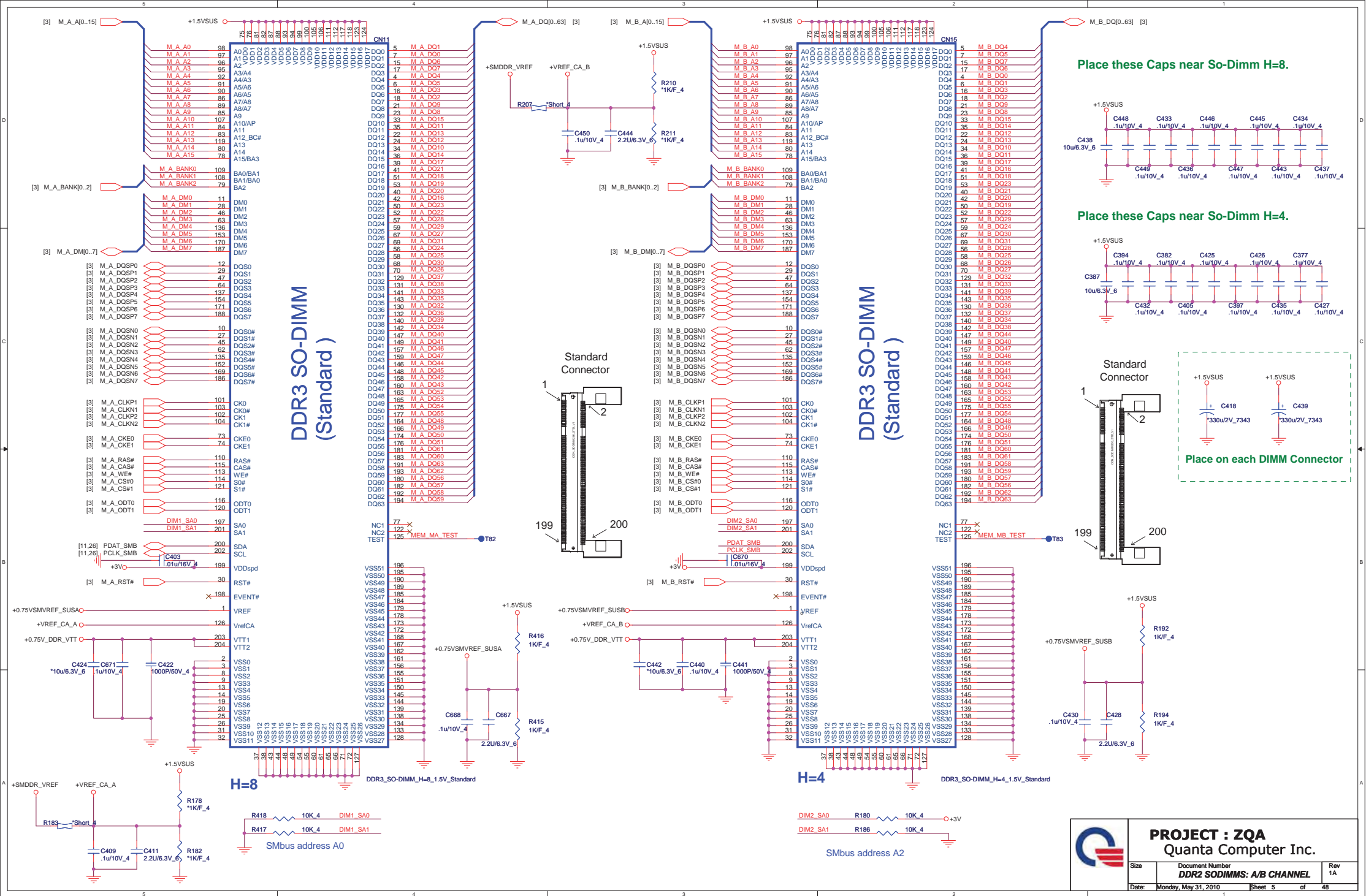


# PROCESSOR POWER AND GROUND



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Size	Document Number <b>S1G4 PWR &amp; GND 3/3</b>	Rev 1A
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[15] PEG\_RXP[15..0] PEG\_RXP[15..0]  
[15] PEG\_RXN[15..0] PEG\_RXN[15..0]

[15] PEG\_TXP[15..0] PEG\_TXP[15..0]  
[15] PEG\_TXN[15..0] PEG\_TXN[15..0]

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

U16B  
PEG\_RXP15 D4  
PEG\_RXN15 C4  
PEG\_RXP14 A3  
PEG\_RXN14 B3  
PEG\_RXP13 C2  
PEG\_RXN13 C1  
PEG\_RXP12 E5  
PEG\_RXN12 F5  
PEG\_RXP11 G5  
PEG\_RXN11 G6  
PEG\_RXP10 H5  
PEG\_RXN10 H6  
PEG\_RXP9 J6  
PEG\_RXN9 J5  
PEG\_RXP8 J7  
PEG\_RXN8 J8  
PEG\_RXP7 L5  
PEG\_RXN7 L6  
PEG\_RXP6 M8  
PEG\_RXN6 L8  
PEG\_RXP5 P7  
PEG\_RXN5 M7  
PEG\_RXP4 P5  
PEG\_RXN4 M5  
PEG\_RXP3 R8  
PEG\_RXN3 P8  
PEG\_RXP2 R6  
PEG\_RXN2 R5  
PEG\_RXP1 P4  
PEG\_RXN1 P3  
PEG\_RXP0 T4  
PEG\_RXN0 T3

PART 2 OF 6

PCIE I/F GFX

GFX\_RX0P  
GFX\_RX0N  
GFX\_RX1P  
GFX\_RX1N  
GFX\_RX2P  
GFX\_RX2N  
GFX\_RX3P  
GFX\_RX3N  
GFX\_RX4P  
GFX\_RX4N  
GFX\_RX5P  
GFX\_RX5N  
GFX\_RX6P  
GFX\_RX6N  
GFX\_RX7P  
GFX\_RX7N  
GFX\_RX8P  
GFX\_RX8N  
GFX\_RX9P  
GFX\_RX9N  
GFX\_RX10P  
GFX\_RX10N  
GFX\_RX11P  
GFX\_RX11N  
GFX\_RX12P  
GFX\_RX12N  
GFX\_RX13P  
GFX\_RX13N  
GFX\_RX14P  
GFX\_RX14N  
GFX\_RX15P  
GFX\_RX15N

A5 PEG\_TXP15 C C568  
B5 PEG\_TXN15 C C570  
A4 PEG\_TXP14 C C561  
B4 PEG\_TXN14 C C562  
C3 PEG\_TXP13 C C557  
B2 PEG\_TXN13 C C559  
D1 PEG\_TXP12 C C553  
D2 PEG\_TXN12 C C556  
E2 PEG\_TXP11 C C549  
F1 PEG\_TXN11 C C552  
F4 PEG\_TXP10 C C541  
E3 PEG\_TXN10 C C548  
F1 PEG\_TXP9 C C537  
F2 PEG\_TXN9 C C540  
H4 PEG\_TXP8 C C527  
H3 PEG\_TXN8 C C536  
H1 PEG\_TXP7 C C535  
H2 PEG\_TXN7 C C539  
J2 PEG\_TXP6 C C518  
J1 PEG\_TXN6 C C525  
K4 PEG\_TXP5 C C523  
K3 PEG\_TXN5 C C526  
K1 PEG\_TXP4 C C530  
K2 PEG\_TXN4 C C529  
M4 PEG\_TXP3 C C522  
M3 PEG\_TXN3 C C521  
M1 PEG\_TXP2 C C532  
M2 PEG\_TXN2 C C531  
N2 PEG\_TXP1 C C520  
N1 PEG\_TXN1 C C519  
P1 PEG\_TXP0 C C534  
P2 PEG\_TXN0 C C533

EV@.1u/10V\_4 PEG\_TXP15  
EV@.1u/10V\_4 PEG\_TXN15  
EV@.1u/10V\_4 PEG\_TXP14  
EV@.1u/10V\_4 PEG\_TXN14  
EV@.1u/10V\_4 PEG\_TXP13  
EV@.1u/10V\_4 PEG\_TXN13  
EV@.1u/10V\_4 PEG\_TXP12  
EV@.1u/10V\_4 PEG\_TXN12  
EV@.1u/10V\_4 PEG\_TXP11  
EV@.1u/10V\_4 PEG\_TXN11  
EV@.1u/10V\_4 PEG\_TXP10  
EV@.1u/10V\_4 PEG\_TXN10  
EV@.1u/10V\_4 PEG\_TXP9  
EV@.1u/10V\_4 PEG\_TXN9  
EV@.1u/10V\_4 PEG\_TXP8  
EV@.1u/10V\_4 PEG\_TXN8  
EV@.1u/10V\_4 PEG\_TXP7  
EV@.1u/10V\_4 PEG\_TXN7  
EV@.1u/10V\_4 PEG\_TXP6  
EV@.1u/10V\_4 PEG\_TXN6  
EV@.1u/10V\_4 PEG\_TXP5  
EV@.1u/10V\_4 PEG\_TXN5  
EV@.1u/10V\_4 PEG\_TXP4  
EV@.1u/10V\_4 PEG\_TXN4  
EV@.1u/10V\_4 PEG\_TXP3  
EV@.1u/10V\_4 PEG\_TXN3  
EV@.1u/10V\_4 PEG\_TXP2  
EV@.1u/10V\_4 PEG\_TXN2  
EV@.1u/10V\_4 PEG\_TXP1  
EV@.1u/10V\_4 PEG\_TXN1  
EV@.1u/10V\_4 PEG\_TXP0  
EV@.1u/10V\_4 PEG\_TXN0

[24] PCIE\_RX1+  
[24] PCIE\_RX1-

AE3  
AD4  
AE2  
AD3

[26] PCIE\_RXP2  
[26] PCIE\_RXN2

AD1  
AD2  
V5  
W6

T33  
T34

U5  
U6  
U8  
U7

[10] A\_RXP0  
[10] A\_RXN0  
[10] A\_RXP1  
[10] A\_RXN1  
[10] A\_RXP2  
[10] A\_RXN2  
[10] A\_RXP3  
[10] A\_RXN3

AA8  
Y8  
AA7  
Y7  
AA5  
AA6  
W5  
Y5

SB\_RX0P  
SB\_RX0N  
SB\_RX1P  
SB\_RX1N  
SB\_RX2P  
SB\_RX2N  
SB\_RX3P  
SB\_RX3N

PCIE I/F GPP

GPP\_RX0P  
GPP\_RX0N  
GPP\_RX1P  
GPP\_RX1N  
GPP\_RX2P  
GPP\_RX2N  
GPP\_RX3P  
GPP\_RX3N  
GPP\_RX4P  
GPP\_RX4N  
GPP\_RX5P  
GPP\_RX5N

AC1 PCIE\_TXP0 C C546  
AC2 PCIE\_TXN0 C C545  
AB4  
AB3  
AA2 PCIE\_TXP2 C C543  
AA1 PCIE\_TXN2 C C544  
Y1  
Y2  
Y4  
Y3  
V1  
V2

.1u/10V\_4  
.1u/10V\_4  
PCIE\_TX1+ [24]  
PCIE\_TX1- [24]  
.1u/10V\_4  
.1u/10V\_4  
PCIE\_TXP2 [26]  
PCIE\_TXN2 [26]

LAN

WLAN

PCIE I/F SB

SB\_TX0P  
SB\_TX0N  
SB\_TX1P  
SB\_TX1N  
SB\_TX2P  
SB\_TX2N  
SB\_TX3P  
SB\_TX3N

AD7 A\_TXP0 C C573  
AE7 A\_TXN0 C C569  
AE6 A\_TXP1 C C560  
AD6 A\_TXN1 C C563  
AB6 A\_TXP2 C C555  
AC6 A\_TXN2 C C558  
AD5 A\_TXP3 C C547  
AE5 A\_TXN3 C C551

.1u/10V\_4  
.1u/10V\_4  
.1u/10V\_4  
.1u/10V\_4  
.1u/10V\_4  
.1u/10V\_4  
.1u/10V\_4  
.1u/10V\_4  
A\_TXP0 [10]  
A\_TXN0 [10]  
A\_TXP1 [10]  
A\_TXN1 [10]  
A\_TXP2 [10]  
A\_TXN2 [10]  
A\_TXP3 [10]  
A\_TXN3 [10]

SB

PCE\_CALRP(PCE\_BCALRP)  
PCE\_CALRN(PCE\_BCALRN)

AC8 NB\_PCIECALRP R326 1.27K/F 4  
AB8 NB\_PCIECALRN R330 2K/F 4  
+1.1V

INT HDMI

PEG\_TXP15 C C76  
PEG\_TXN15 C C78  
PEG\_TXP14 C C73  
PEG\_TXN14 C C75  
PEG\_TXP13 C C68  
PEG\_TXN13 C C71  
PEG\_TXP12 C C64  
PEG\_TXN12 C C67

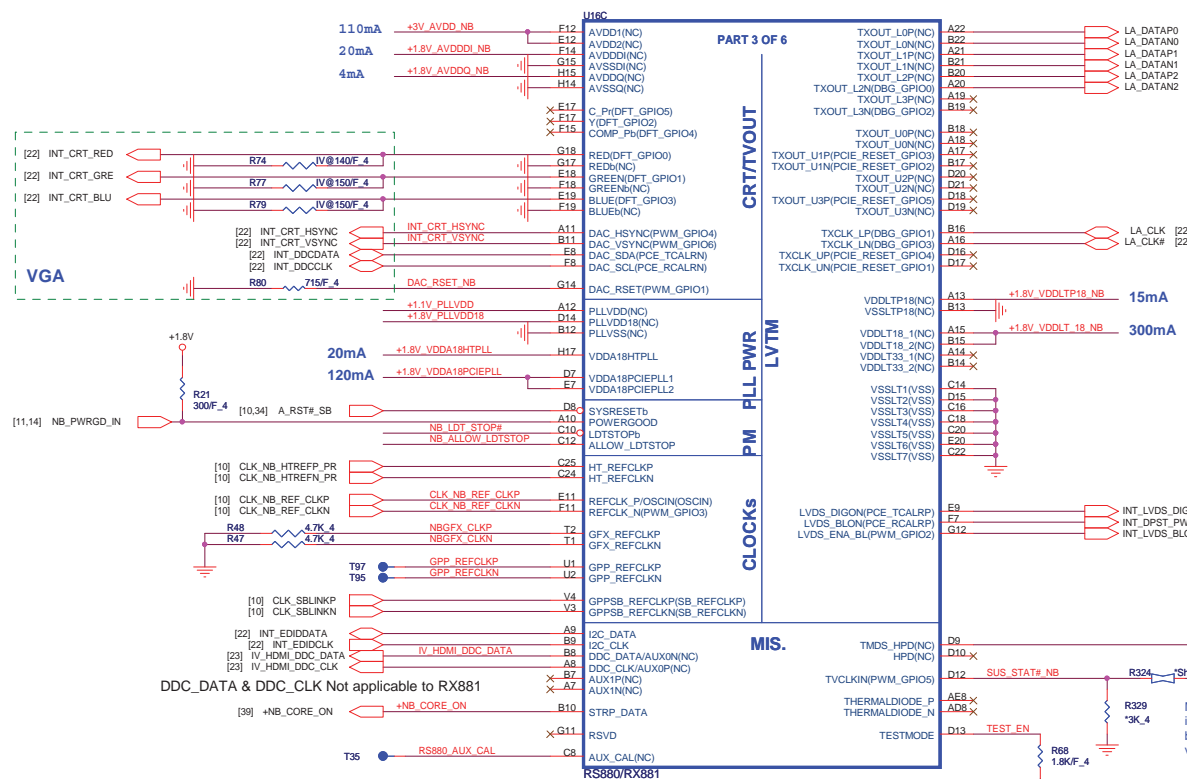
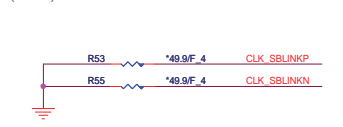
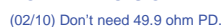
IV@.1u/10V\_4  
IV@.1u/10V\_4  
IV@.1u/10V\_4  
IV@.1u/10V\_4  
IV@.1u/10V\_4  
IV@.1u/10V\_4  
IV@.1u/10V\_4  
IV@.1u/10V\_4  
IV\_TX2\_HDMI+ [23]  
IV\_TX2\_HDMI- [23]  
IV\_TX1\_HDMI+ [23]  
IV\_TX1\_HDMI- [23]  
IV\_TX0\_HDMI+ [23]  
IV\_TX0\_HDMI- [23]  
IV\_TXC\_HDMI+ [23]  
IV\_TXC\_HDMI- [23]



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R325 \*4.7K\_4 NB\_PWRGD\_IN  
 +3V R59 \*4.7K\_4 INT\_EDIDDATA  
 R60 \*4.7K\_4 INT\_EDIDCLK  
 +3V R58 \*4.7K\_4 IV\_HDMI\_DDC\_DATA



Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	V
0 Enable	

```
RS880M:INT CRT HSYNC
```

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

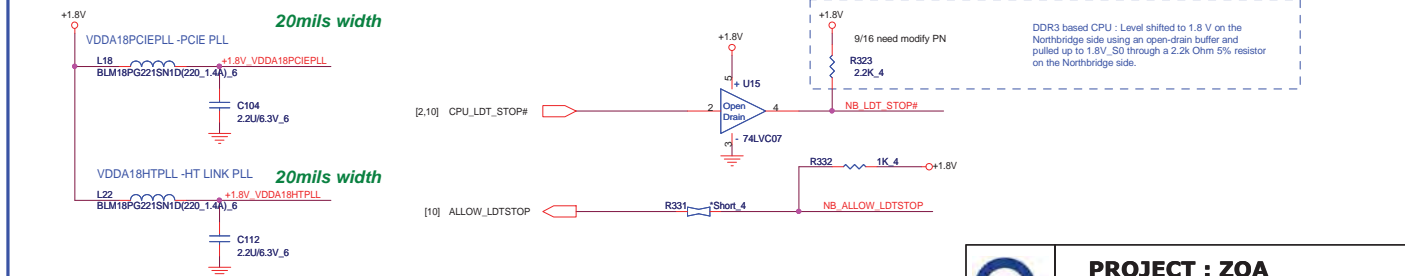
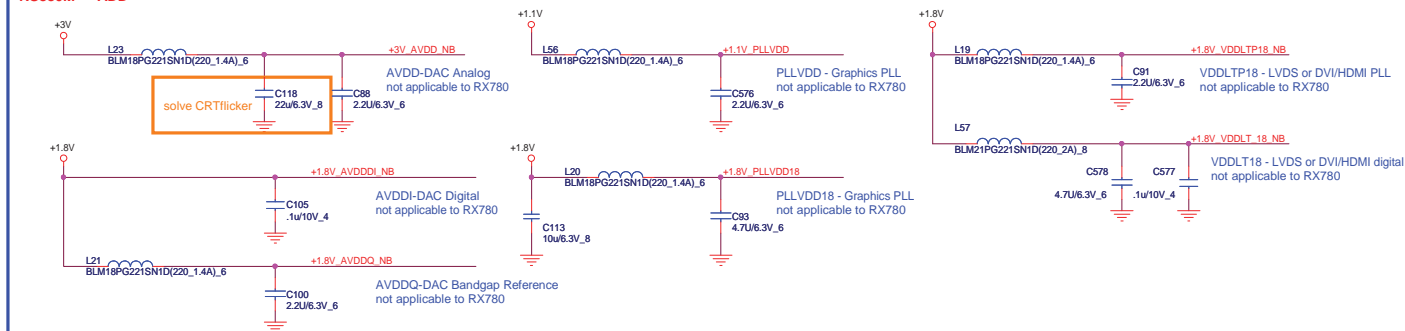
Register Readback of strap: NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]



## RS780/RX780/RS880



**Display Port interface from PCIeGraphics (RS880/rs880M only)**



The RS880 family does not support CLMC architecture  
The LDTREQ# connection from the CPU to ALLOW\_LDTSTOP  
of the Northbridge is no longer required.



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Size	Document Number <b>RS880M-SYSTEM I/F 3/4</b>	Rev 1A
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The diagram shows three resistors connected to a common +3V\_S5 supply. The resistors are labeled R271, R32, and R28, each with a value of \*2.2K 4. They are connected to test points SB\_TEST0, SB\_TEST1, and SB\_TEST2 respectively.

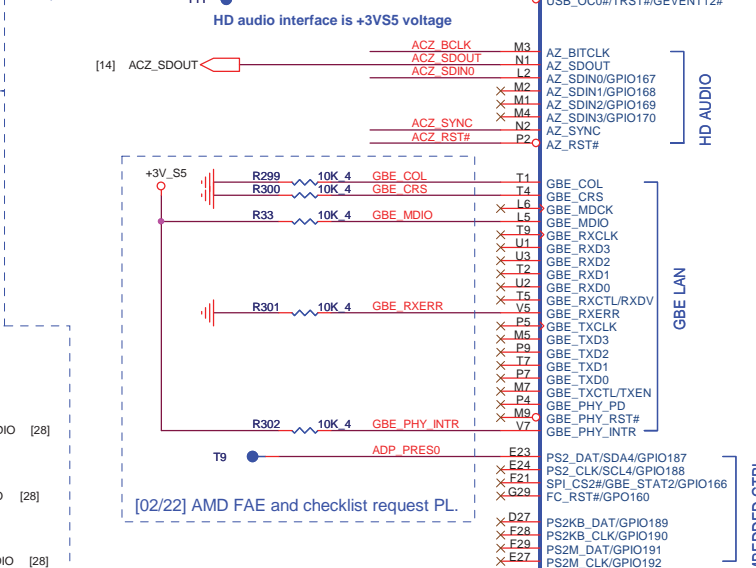
+3V\_S5

R23 10K 4 SB\_SCLK2  
R22 10K 4 SB\_SDATA2

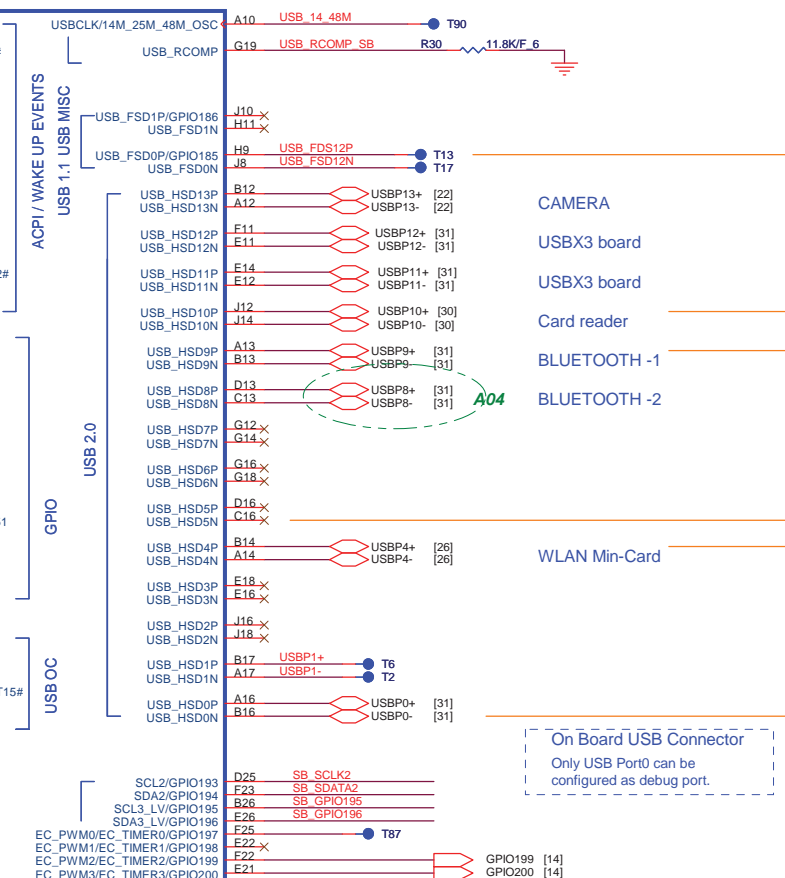
+3V

R31 4.7K 4 SUS\_STAT#

Signal	Resistor	Voltage Divider	Capacitor	Audio Pin
ACZ_SDOUT	R294	33 k / 4 k	*10P/50V 4	ACZ_SDOUT_AUDIO [28]
ACZ_SYNC	R295	33 k / 4 k	*10P/50V 4	ACZ_SYNC_AUDIO [28]
ACZ_BCLK	R291	33 k / 4 k	*10P/50V 4	ACZ_BITCLK_AUDIO [28]
ACZ_RST#	R298	33 k / 4 k	*10P/50V 4	ACZ_RST#_AUDIO [28]
ACZ_SDI0				ACZ_SDI0 [28]



USBCLK/41M\_25M\_48M\_OSC pin is CLK input pin when EXT CLKGEN mode.  
It is output CLK source when INT CLKGEN mode.



SB\_GPIO195 R284 10K\_4

SB\_GPIO196 R283 10K\_4



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Size	Document Number <b>SB820-ACPI/GPIO/USB 2/4</b>	Rev 1A
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Max trace length: 6"

### SATA HDD



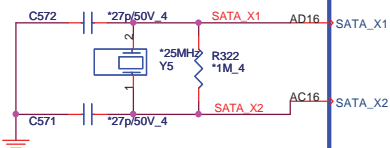
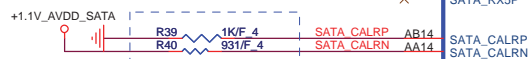
## SATA ODD



**SATA PORT 0,1,2,3 can support AHCI mode**

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

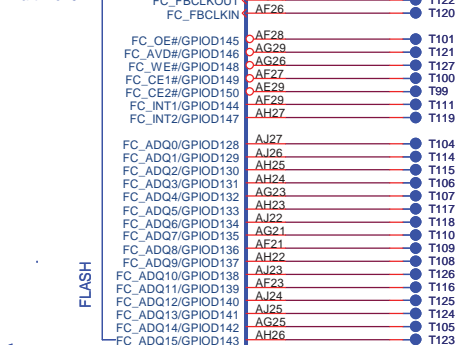
## E-SATA



PLACE SATA\_CAL  
RES VERY CLOSE  
TO BALL OF SB820

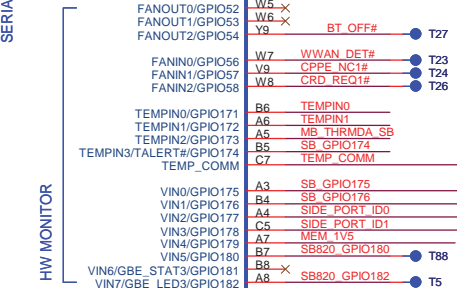
**SB800**

Part 2 of 5



IF THERE IS NO IDE, TEST POINTS FOR  
DEBUG BUS IS MANDATORY

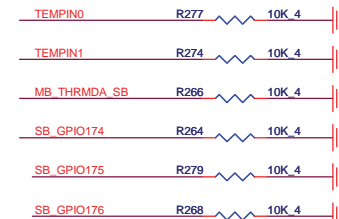
SERIAL ATA



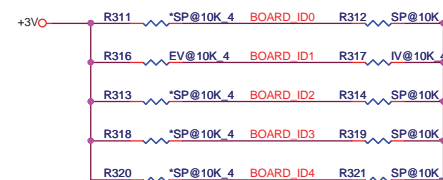
1  
 2  
 3  
 4  
 5



## Check list

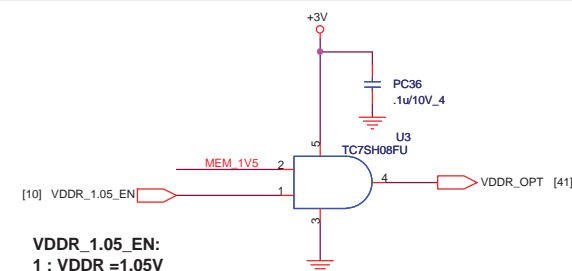


## BOM check



	1	0
ID0		
ID1	DIS	UM
ID2		
ID3		
ID4		

- |      |           |           |
|------|-----------|-----------|
| [10] | BOARD_ID0 | BOARD ID0 |
| [10] | BOARD_ID1 | BOARD ID1 |
| [10] | BOARD_ID2 | BOARD ID2 |
| [10] | BOARD_ID3 | BOARD ID3 |
| [10] | BOARD_ID4 | BOARD ID4 |



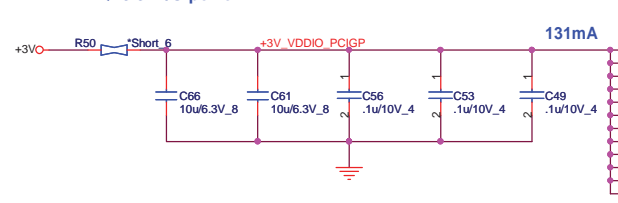
**VDDR\_1.05\_EN:**  
1 : VDDR =1.05V  
0 : VDDR = 0.9V (Default)



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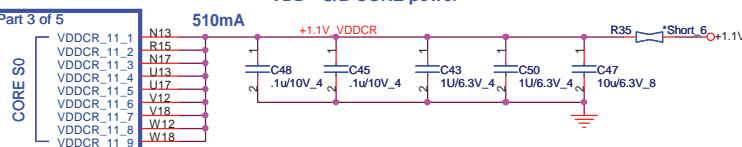
Size	Document Number <b>SB820-SATA/IDE/SPI 3/4</b>	Rev 1A
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## VDDQ--3.3V I/O power

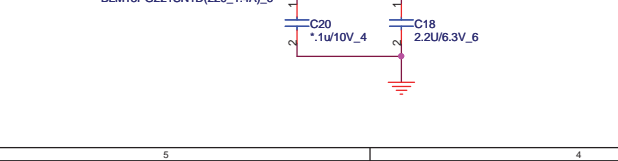
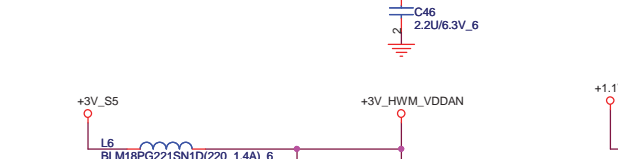
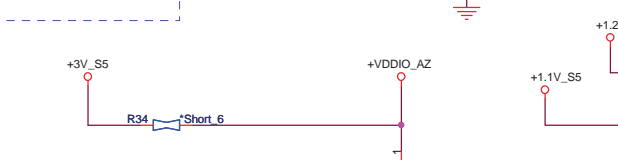
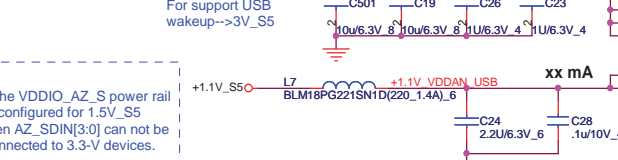
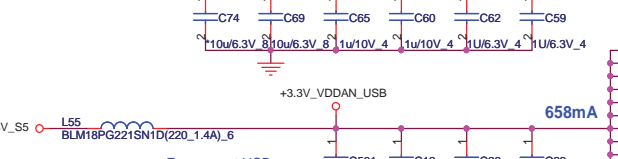
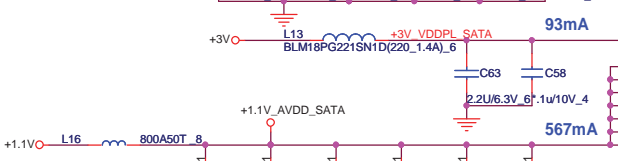
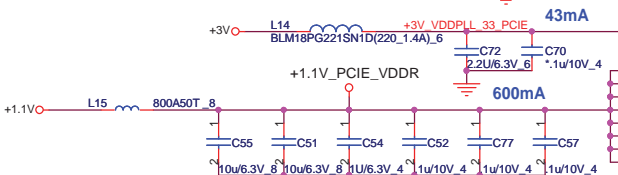


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

## VDD-- S/B CORE power



## POWER



## FLASH I/O

## VDDIO\_18\_FC\_1

## VDDIO\_18\_FC\_2

## VDDIO\_18\_FC\_3

## VDDIO\_18\_FC\_4

## VDDPL\_33\_PCIE

## VDDAN\_11\_PCIE\_1

## VDDAN\_11\_PCIE\_2

## VDDAN\_11\_PCIE\_3

## VDDAN\_11\_PCIE\_4

## VDDAN\_11\_PCIE\_5

## VDDAN\_11\_PCIE\_6

## VDDAN\_11\_PCIE\_7

## VDDAN\_11\_PCIE\_8

## VDDPL\_33\_SATA

## VDDAN\_11\_SATA\_1

## VDDAN\_11\_SATA\_2

## VDDAN\_11\_SATA\_3

## VDDAN\_11\_SATA\_4

## VDDAN\_11\_SATA\_5

## VDDAN\_11\_SATA\_6

## VDDAN\_11\_SATA\_7

## VDDAN\_11\_SATA\_8

## VDDAN\_33\_USB\_S\_1

## VDDAN\_33\_USB\_S\_2

## VDDAN\_33\_USB\_S\_3

## VDDAN\_33\_USB\_S\_4

## VDDAN\_33\_USB\_S\_5

## VDDAN\_33\_USB\_S\_6

## VDDAN\_33\_USB\_S\_7

## VDDAN\_33\_USB\_S\_8

## VDDAN\_33\_USB\_S\_9

## VDDAN\_33\_USB\_S\_10

## VDDAN\_33\_USB\_S\_11

## VDDAN\_33\_USB\_S\_12

## VDDAN\_11\_USB\_S\_1

## VDDAN\_11\_USB\_S\_2

## VDDAN\_33\_HWM\_S

## VDDXL\_33\_S

## VDDIO\_AZ

## VDDIO\_18\_FC\_1

## VDDIO\_18\_FC\_2

## VDDIO\_18\_FC\_3

## VDDIO\_18\_FC\_4

## VDDRF\_GBE\_S

## VDDIO\_33\_GBE\_S

## VDDCR\_11\_GBE\_S\_1

## VDDCR\_11\_GBE\_S\_2

## VDDIO\_GBE\_S\_1

## VDDIO\_GBE\_S\_2

## VDDIO\_33\_S\_1

## VDDIO\_33\_S\_2

## VDDIO\_33\_S\_3

## VDDIO\_33\_S\_4

## VDDIO\_33\_S\_5

## VDDIO\_33\_S\_6

## VDDIO\_33\_S\_7

## VDDIO\_33\_S\_8

## VDDIO\_33\_S\_9

## VDDIO\_33\_S\_10

## VDDIO\_33\_S\_11

## VDDIO\_33\_S\_12

## VDDIO\_33\_S\_13

## VDDIO\_33\_S\_14

## VDDIO\_33\_S\_15

## VDDIO\_33\_S\_16

## VDDIO\_33\_S\_17

## VDDIO\_33\_S\_18

## VDDIO\_33\_S\_19

## VDDIO\_33\_S\_20

## VDDIO\_33\_S\_21

## VDDIO\_33\_S\_22

## VDDIO\_33\_S\_23

## VDDIO\_33\_S\_24

## VDDIO\_33\_S\_25

## VDDIO\_33\_S\_26

## VDDIO\_33\_S\_27

## VDDIO\_33\_S\_28

## VDDIO\_33\_S\_29

## VDDIO\_33\_S\_30

## VDDIO\_33\_S\_31

## VDDIO\_33\_S\_32

## VDDIO\_33\_S\_33

## VDDIO\_33\_S\_34

## VDDIO\_33\_S\_35

## VDDIO\_33\_S\_36

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## VDDIO\_33\_S\_162

## VDDIO\_33\_S\_163

## VDDIO\_33\_S\_164

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## VDDIO\_33\_S\_187

## VDDIO\_33\_S\_188

## VDDIO\_33\_S\_189

## VDDIO\_33\_S\_190

## VDDIO\_33\_S\_191

## VDDIO\_33\_S\_192

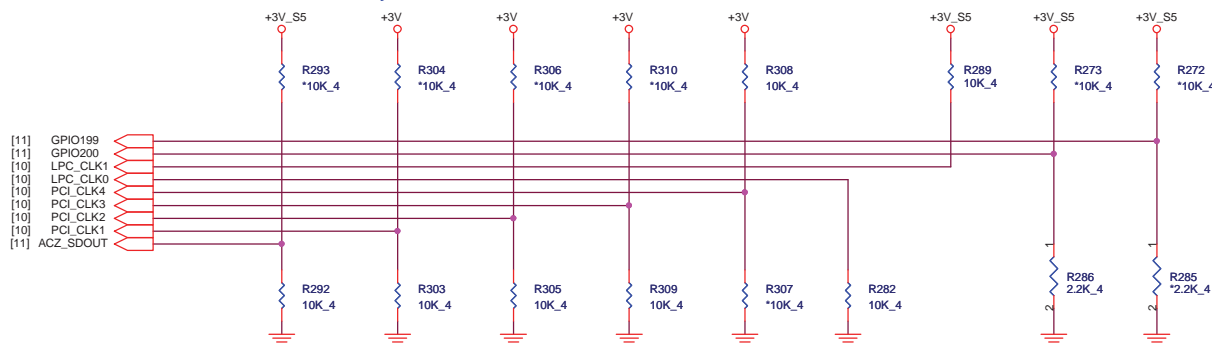
## VDDIO\_33\_S\_193



## REQUIRED STRAPS

SB820M is supported Gen.1 mode only.

For internal clock GEN.

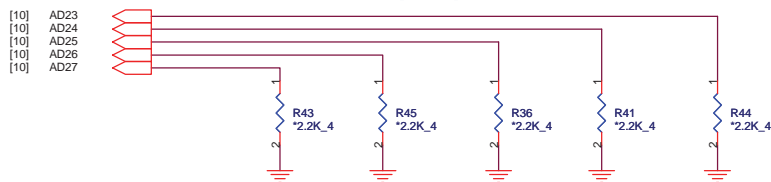


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM	DEFAULT

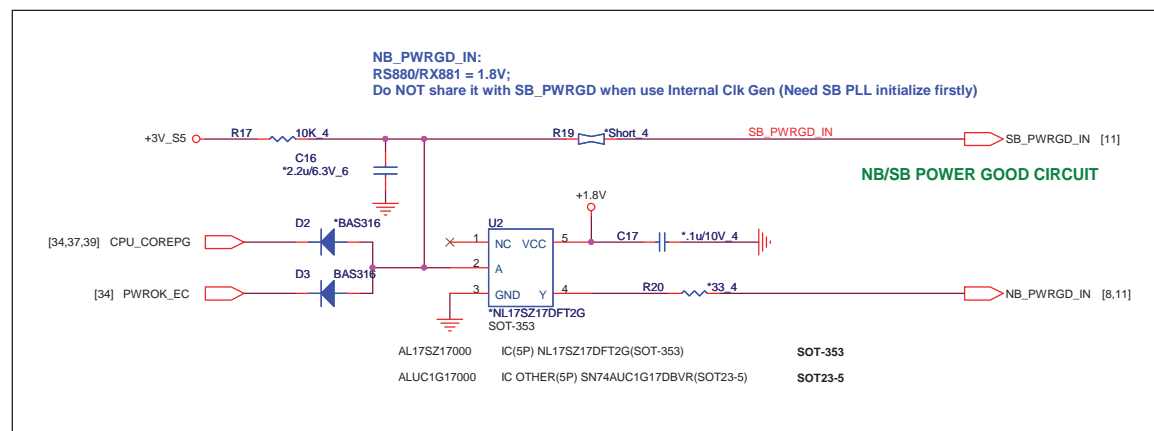
internal have pull Hi 10K

## DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

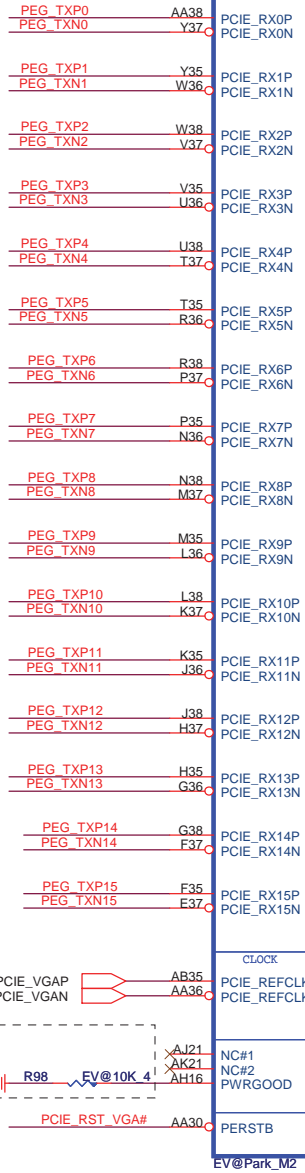
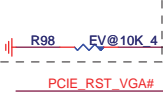
14



PROJECT : ZQA  
Quanta Computer Inc.

Size	Document Number <b>SB820-STRAPS</b>	Rev 1A
Date: Monday, May 31, 2010	Sheet 14	of 48

U20A

[7] PEG\_TXP[15..0]  PEG\_TXP[15..0][7] PEG\_TXN[15..0]  PEG\_TXN[15..0][7] PEG\_RXP[15..0]  PEG\_RXP[15..0][7] PEG\_RXN[15..0]  PEG\_RXN[15..0][10] CLK\_PCIE\_VGAP  
[10] CLK\_PCIE\_VGANFor Madison and Park  
the PWRGOOD ball must  
be connected to ground

PCI EXPRESS INTERFACE

CALIBRATION

PCIE\_CALRP

PCIE\_CALRN

NC#1

NC#2

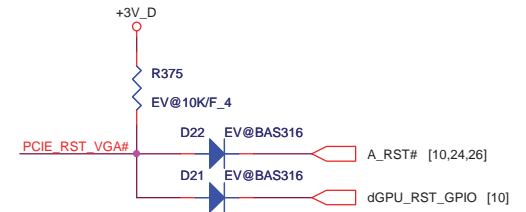
PWRGOOD

PERSTB

EV@Park\_M2



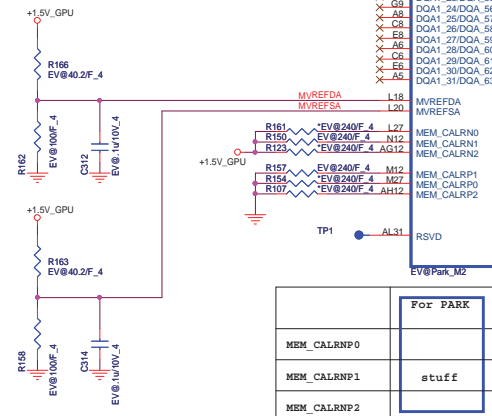
For Madison and Park PCIE\_VDDC is 1.0V



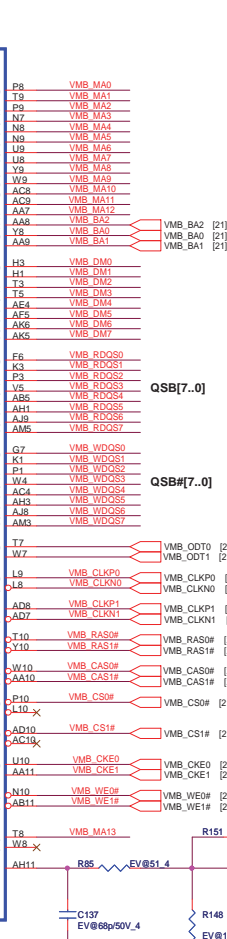
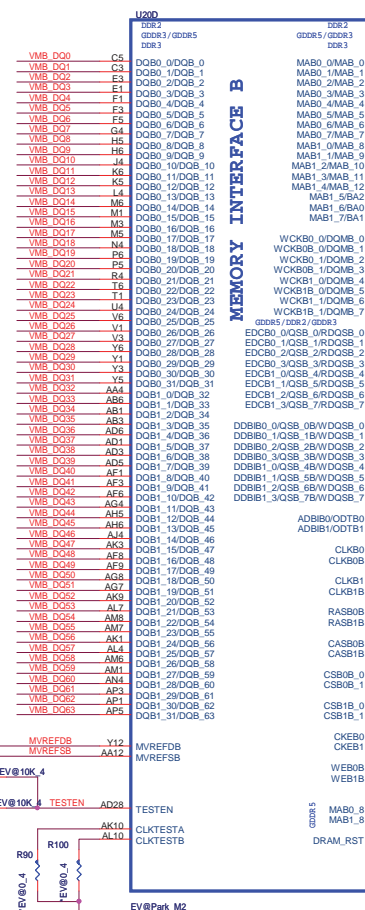
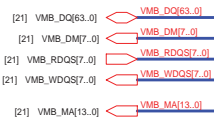
**PROJECT : ZQA**  
Quanta Computer Inc.

Size	Document Number <b>Madison/Park-PCIE 1/6</b>	Rev 1A
Date: Monday, May 31, 2010	Sheet 15 of 48	





	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Designator	For M97-M2	For Mannhatten
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF



**PROJECT : ZQA**  
Quanta Computer Inc.

Size	Document Number	Revisions
	<b>Madison/Park-MEM 3/6</b>	1A
Date:	Monday, May 31, 2010	Sheet 17 of 48

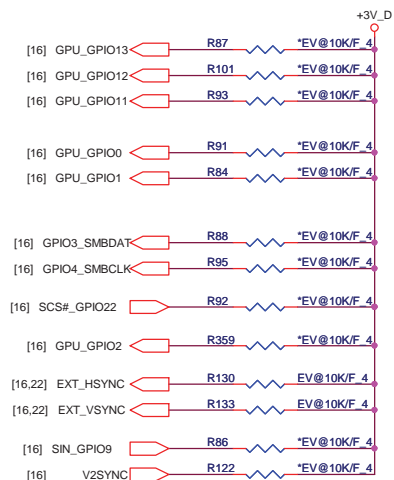






**NOTE : DPD is NA on Park,Robson and Seymour.**

## PIN STRAPS



## Memory Aperture size

GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

## ROM Table

EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

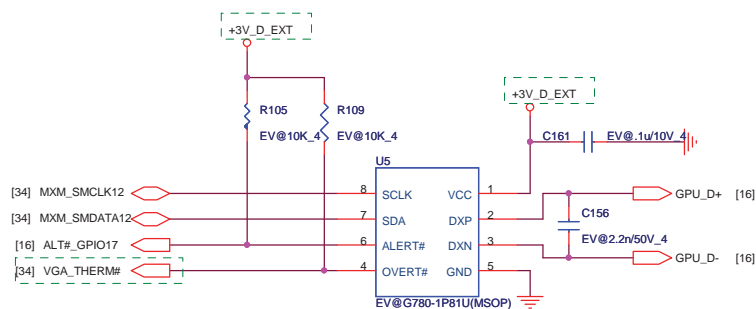
20

## DDR3 Memory Aperture size

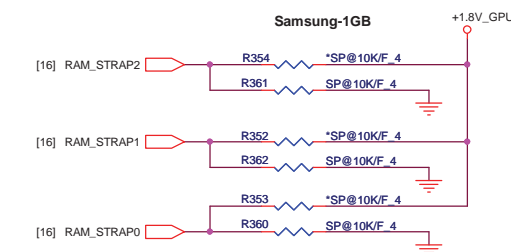
## DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVDPDATA_2	RAM_STRAP1 DVDPDATA_1	RAM_STRAP0 DVDPDATA_0
Hynix			512MB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	1	0	0
			2GB	1	1	1
Samsung			512MB	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1


## Thermal Sensor



Address ID: 98H

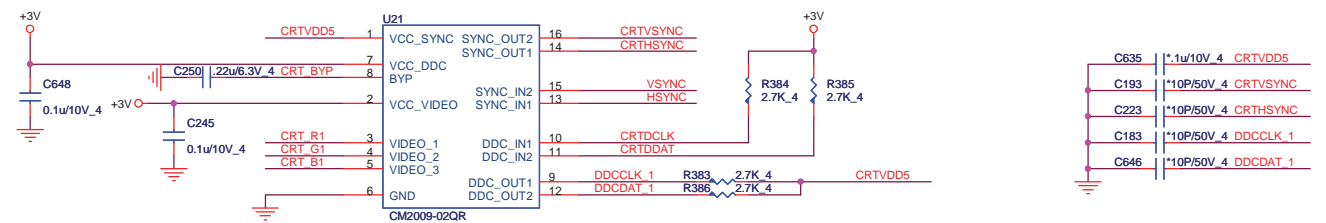
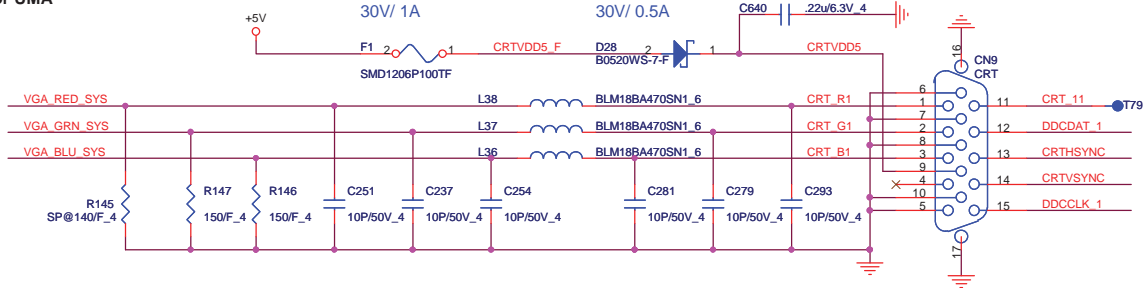
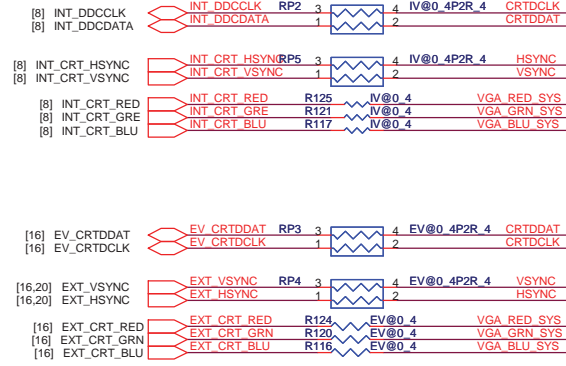


RAM\_STRAP2 SET DDR3 Vendor  
RAM\_STRAP[1:0] SET SIZE.

 <b>PROJECT : ZQA</b> Quanta Computer Inc.		
Size	Document Number <b>Medison/Park Strip/Thermal 6/6</b>	Rev 1A
Date:	Monday, May 31, 2010	Sheet 20 of 48

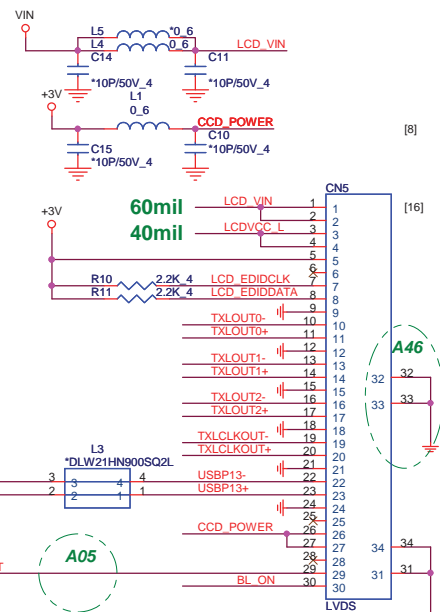
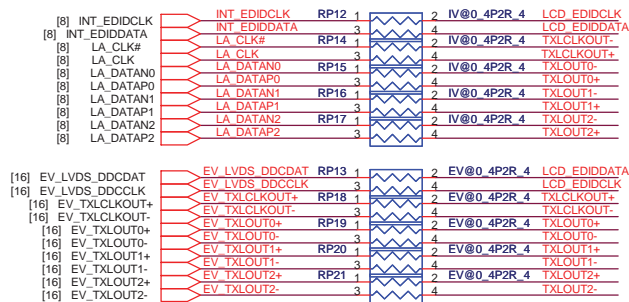


OPTION SIGNAL FROM NB to CRT for UMA

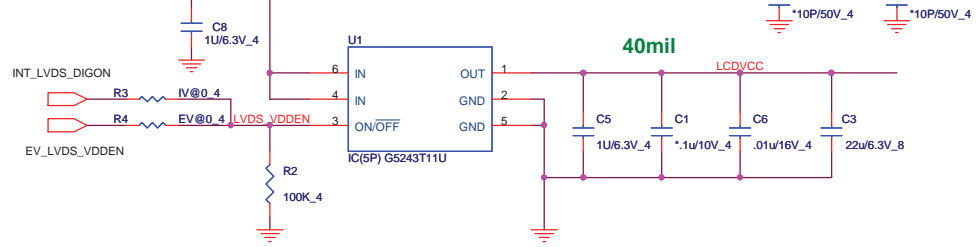


OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA

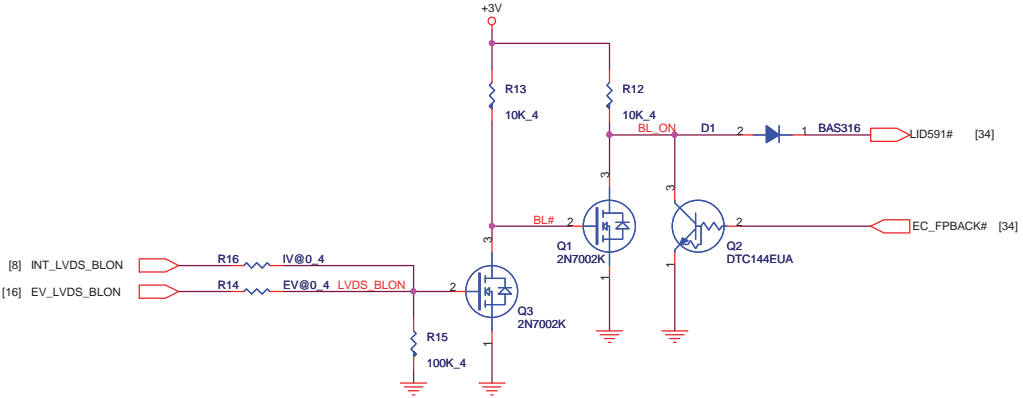
LVDS(LDS) OPTION SIGNAL FROM NB to LVDS for UMA



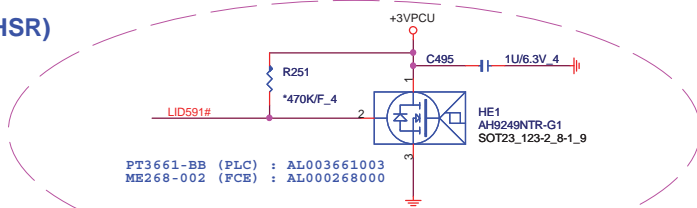
LCD PW(LDS)



Backlight Control(LDS)



Lid Switch (HSR)



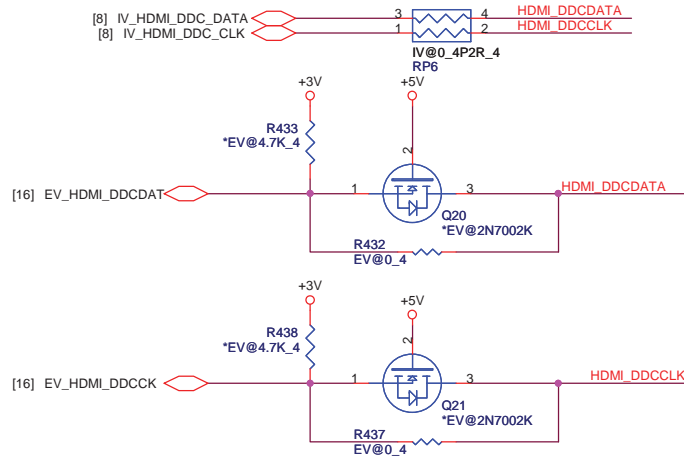
PT3661-BB (PLC) : AL003661003  
ME268-002 (FCE) : AL000268000

## HDMI SDVO I2C Control

UMA

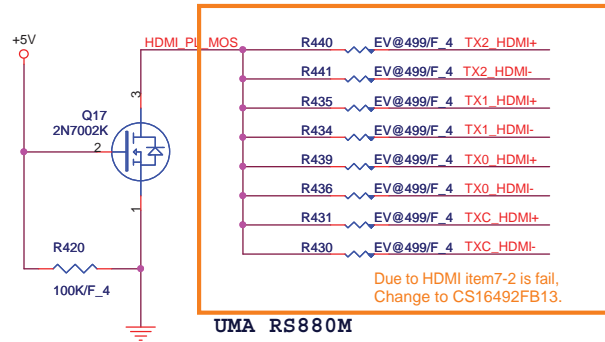
Close to HDMI Connector

DIS



HDMI (HDM)

Close to HDMI Connector



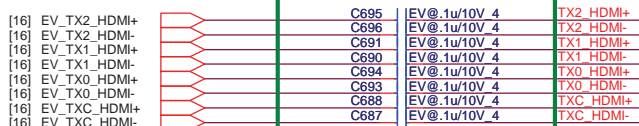
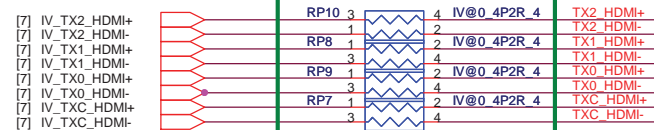
UMA RS880M

Stuff 715 ohm CS17152FB17

DIS Park-M2

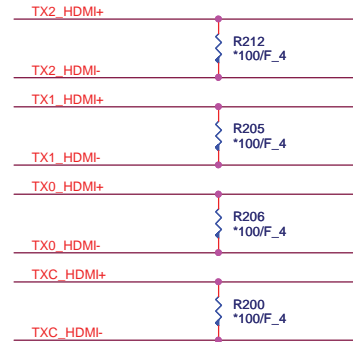
Stuff 499 ohm CS14992FB24

for Layout concern  
,placement close HDMI conn

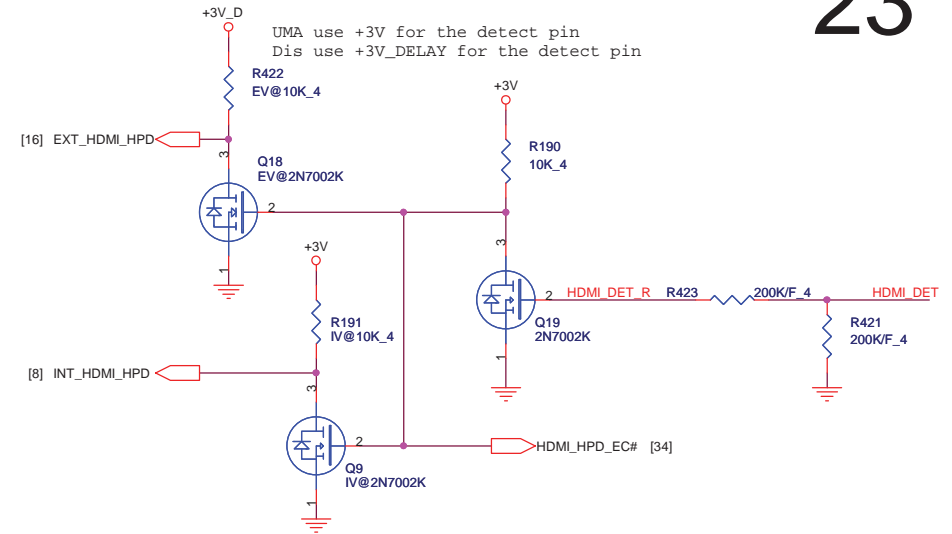


EMI reserve for HDMI(EMC)

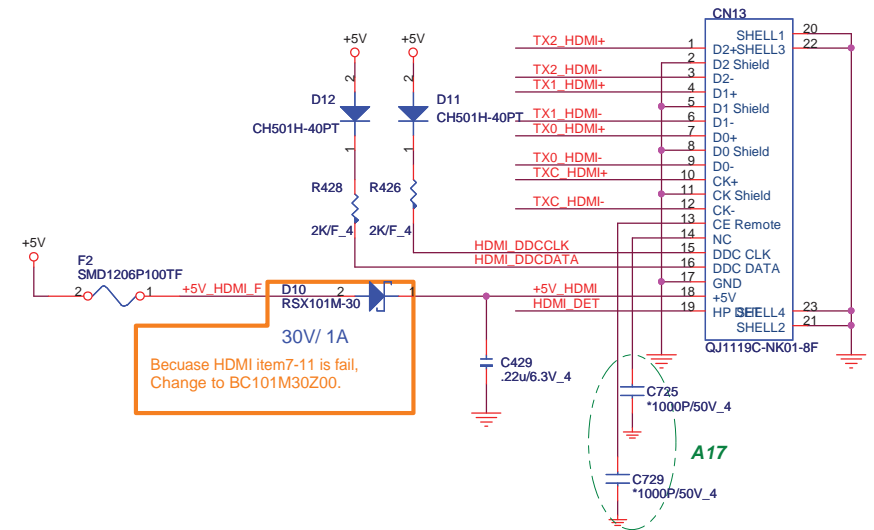
Close connector



## HDMI HPD SENSE (HDM)



HDMI PORT (HDM)

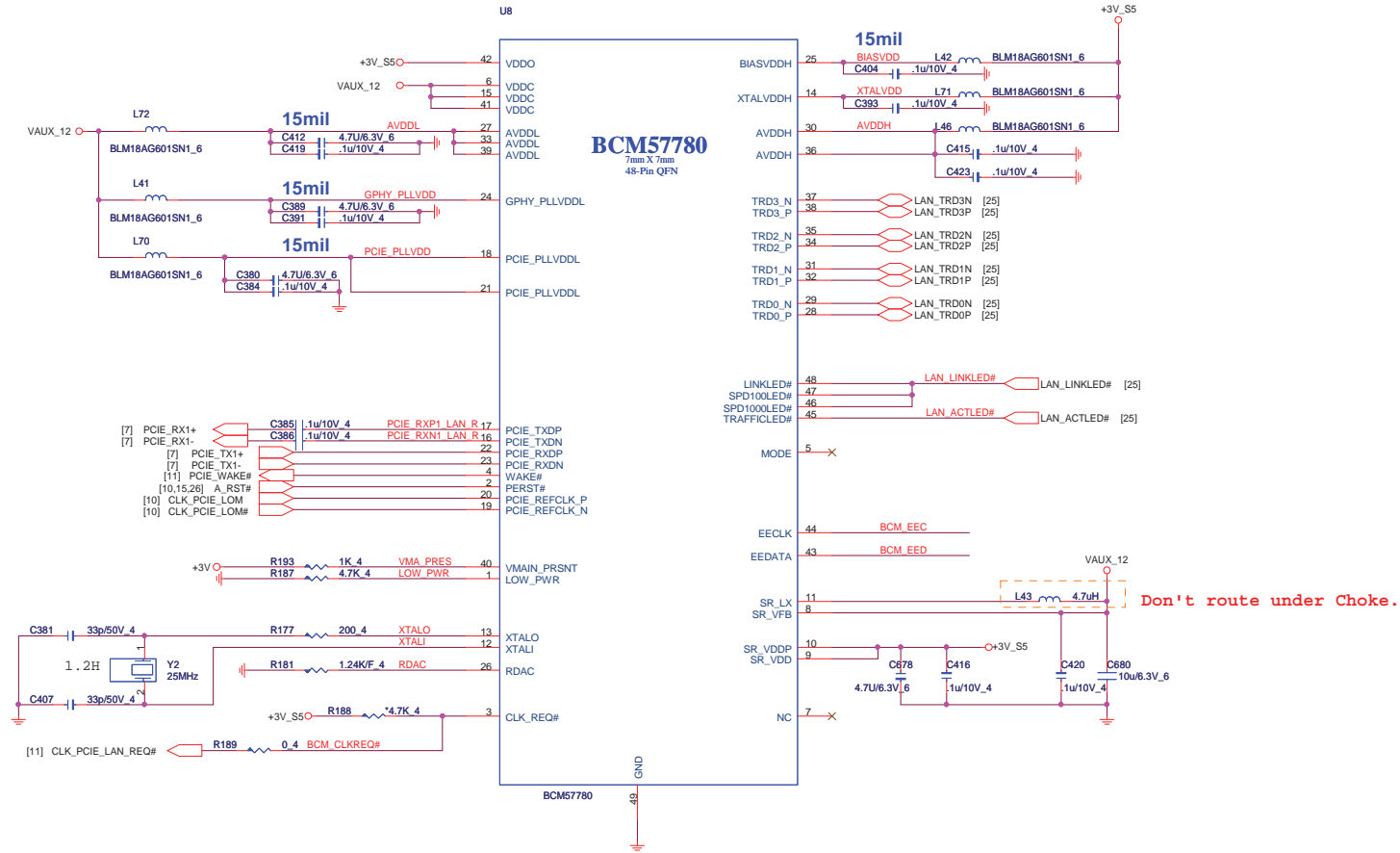


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**Quanta Computer Inc.**

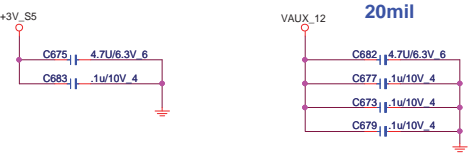
Size	Document Number	Rev
	<b>HDMI</b>	1A
Date:	Monday, May 31, 2010	Sheet 23 of 48

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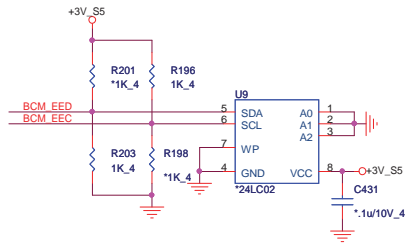




LAN POWER



EEPROM

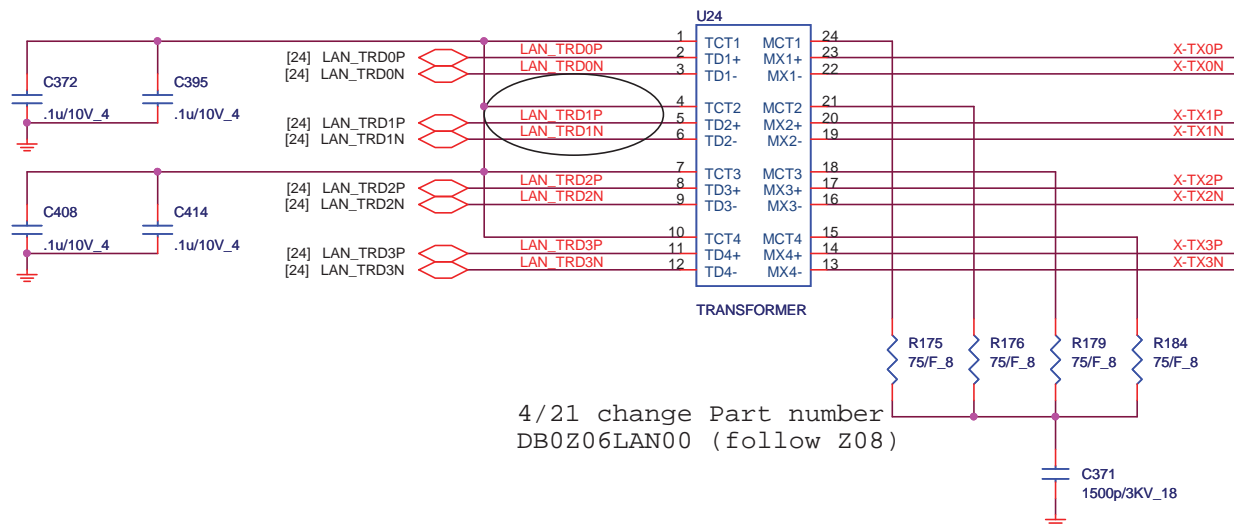


EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

## TRANSFORMER

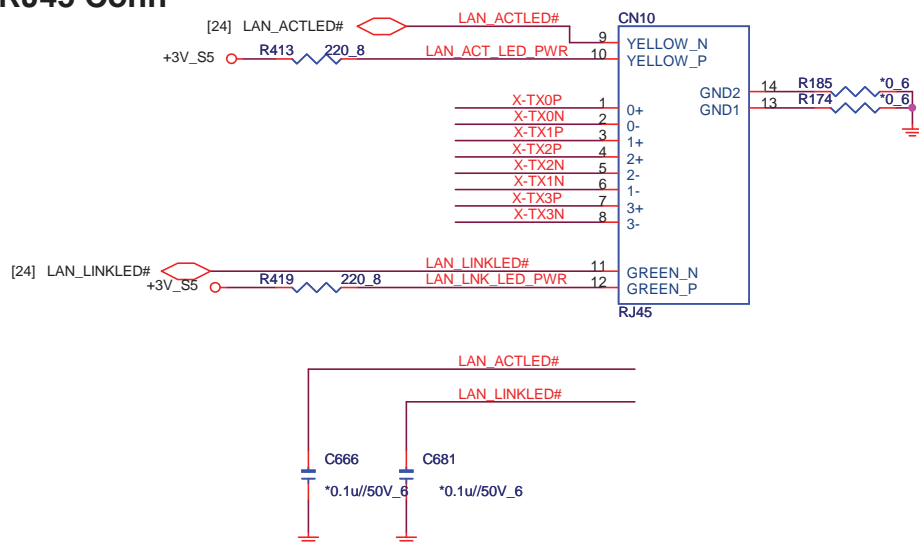
4/27 modify it



4/21 change Part number  
DB0Z06LAN00 (follow Z08)

For EMI

## RJ45 Conn



LAN_TRD0P	C378	*10P/50V_4
LAN_TRD0N	C388	*10P/50V_4
LAN_TRD1P	C399	*10P/50V_4
LAN_TRD1N	C402	*10P/50V_4
LAN_TRD2P	C410	*10P/50V_4
LAN_TRD2N	C413	*10P/50V_4
LAN_TRD3P	C417	*10P/50V_4
LAN_TRD3N	C421	*10P/50V_4



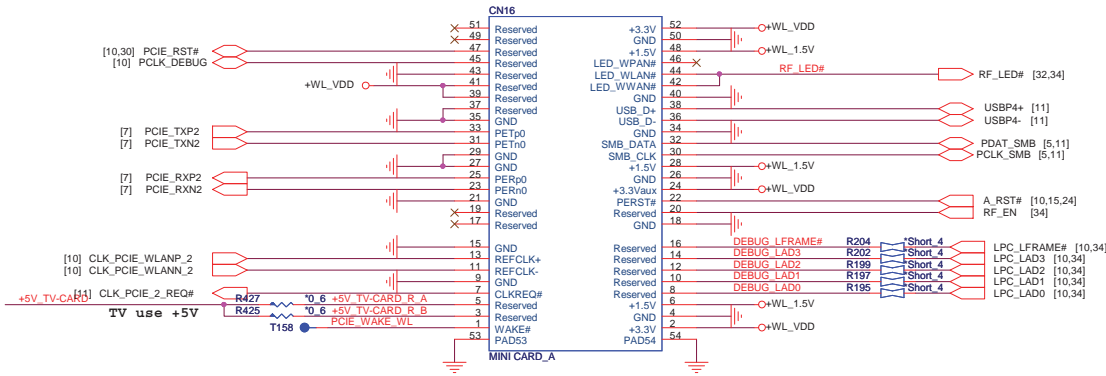
**PROJECT : ZQA**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>LAN Transformer and RJ45</b>	1A
Date:	Monday, May 31, 2010	Sheet 25 of 48

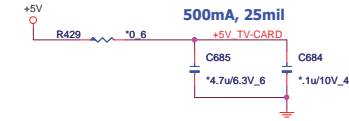
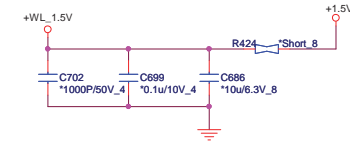
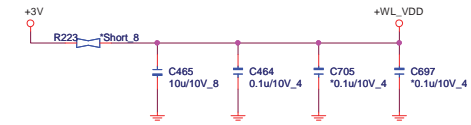
# MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

Check LED signal. (active high or low)



Debug



26

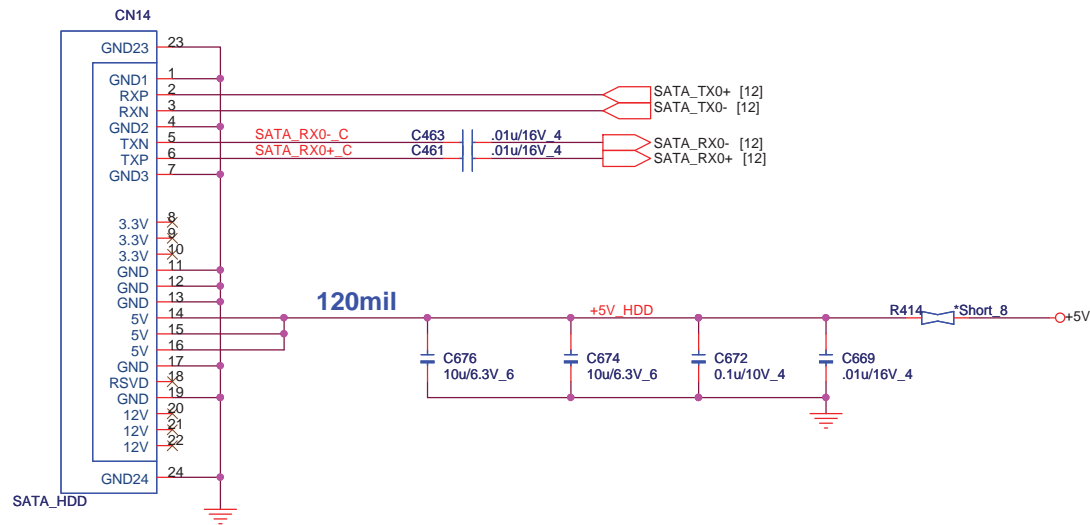


**PROJECT : ZQA**  
Quanta Computer Inc.

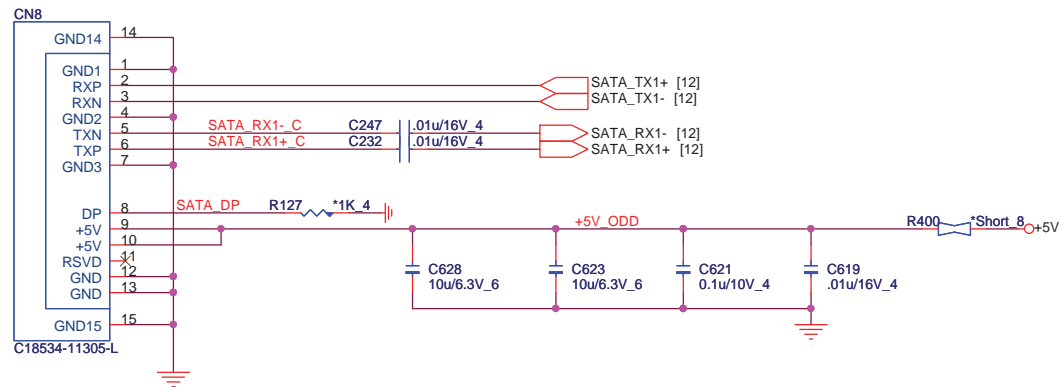
Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date: Monday, May 31, 2010	Sheet 26 of 48	


# SATA HDD

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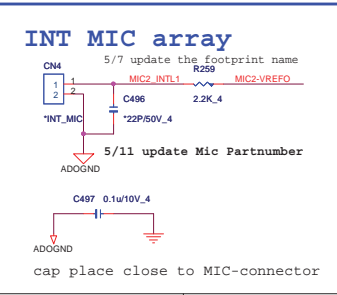
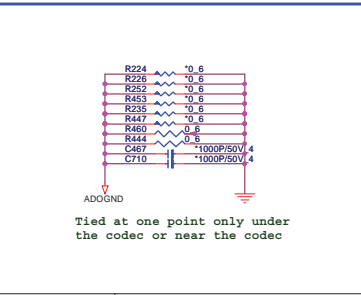
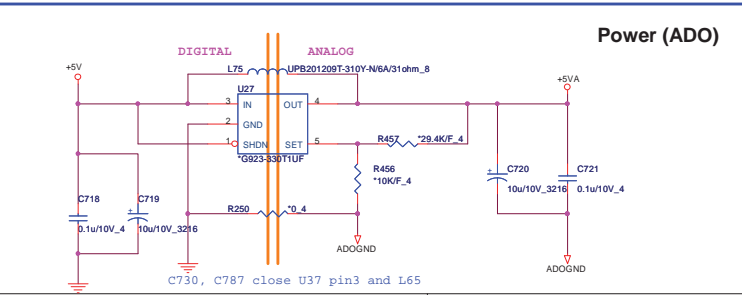
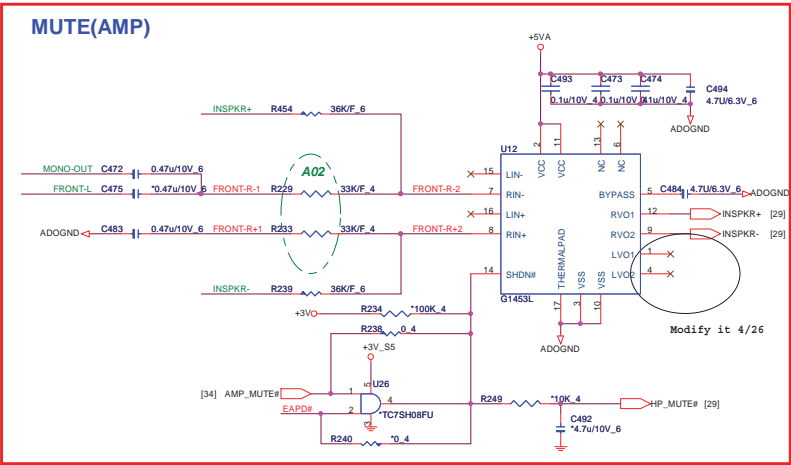
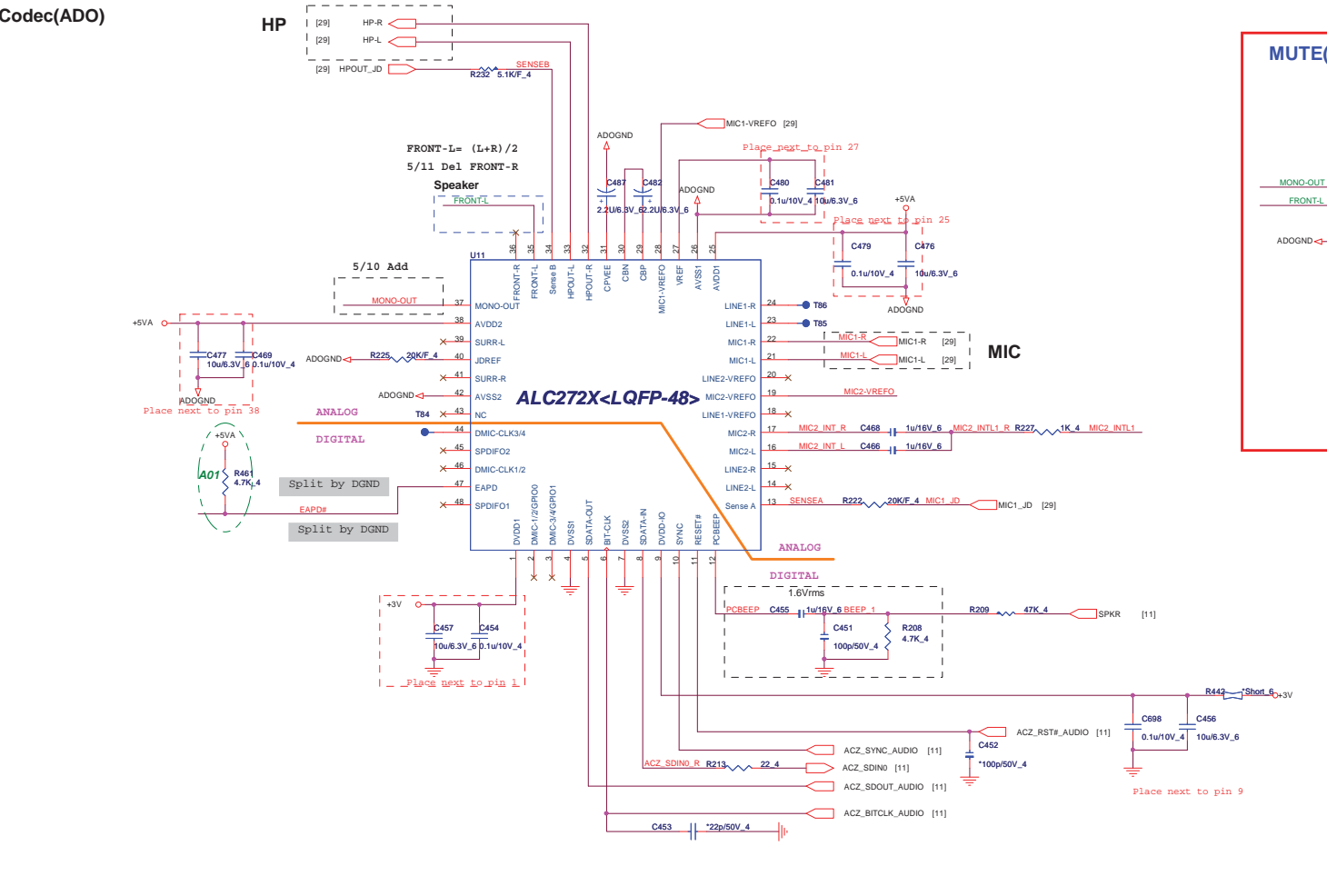



# SATA ODD



			<b>PROJECT : ZQA</b> Quanta Computer Inc.	
Size	Document Number <b>SATA-HDD/ODD/HOLE</b>		Rev 1A	
Date:	Monday, May 31, 2010	Sheet	27 of 48	

Codec(ADO)



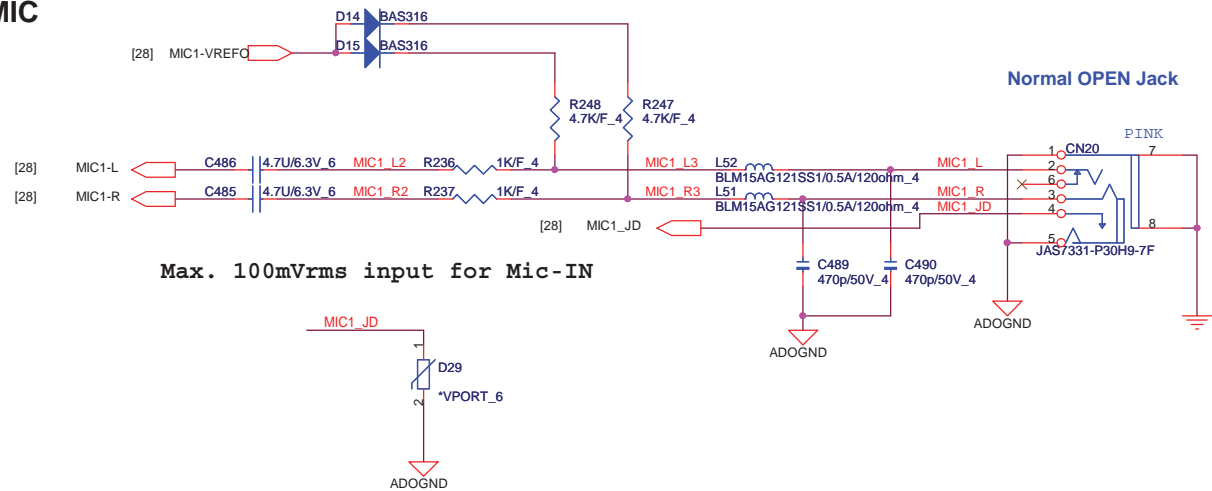


**PROJECT : ZQA**  
Quanta Computer Inc.

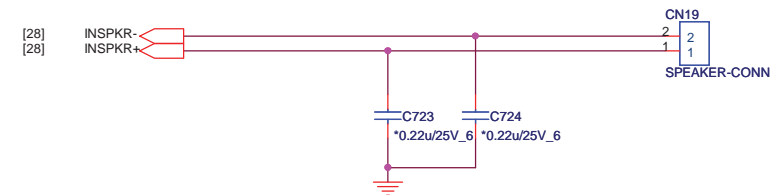
Size	Document Number	Rev
	REALTEK ALC663&888/MDC	1A
Date:	Monday, May 31, 2010	Sheet 28 of 48



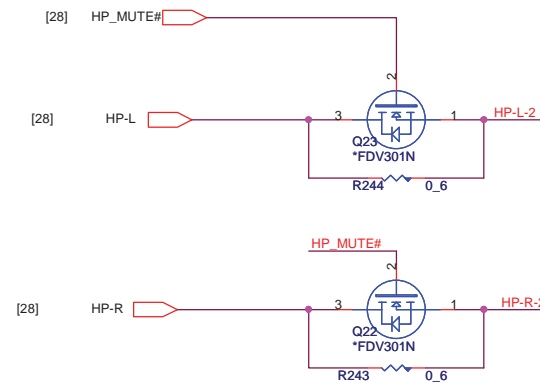
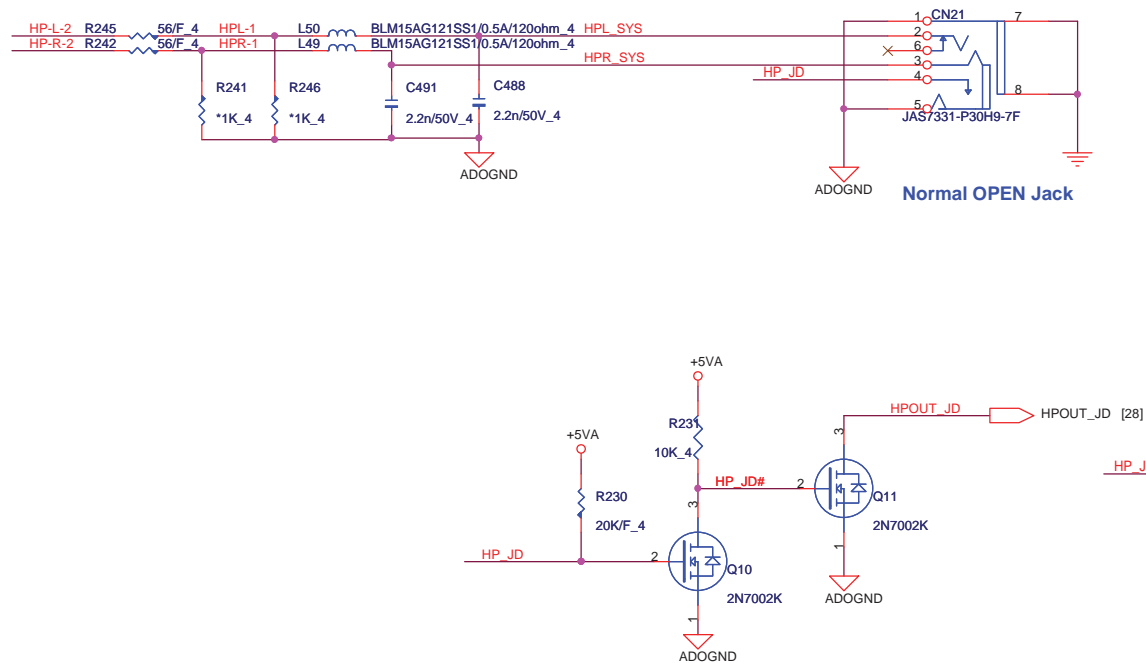
# MIC




# Internal Speaker



# HP



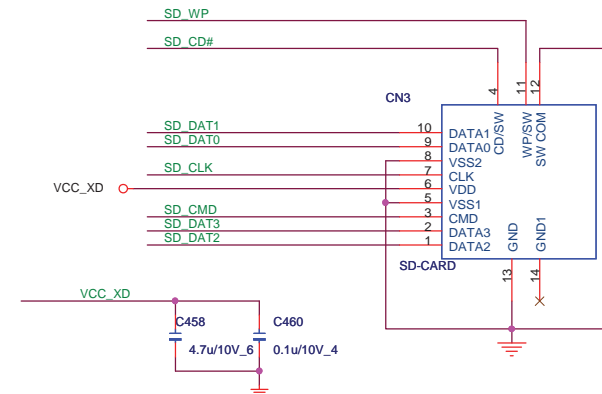
 <b>PROJECT : ZQA</b> Quanta Computer Inc.		
Size	Document Number <b>AMP /AUDIO JACK CONN</b>	Rev 1A
Date:	Monday, May 31, 2010	Sheet 29 of 48

## CARD READER Controller

## 2 IN 1 CARD READER (MMC)

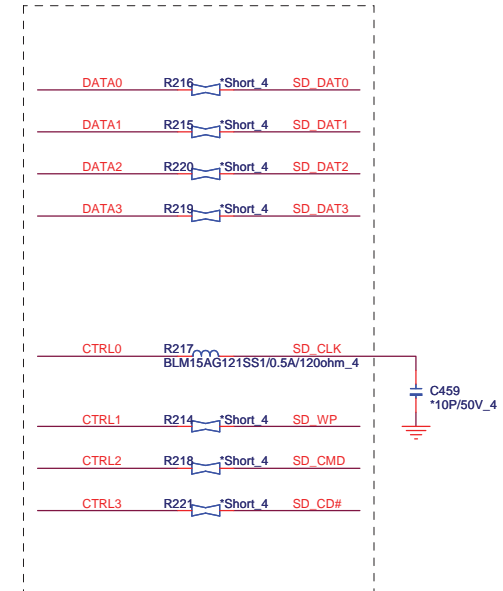
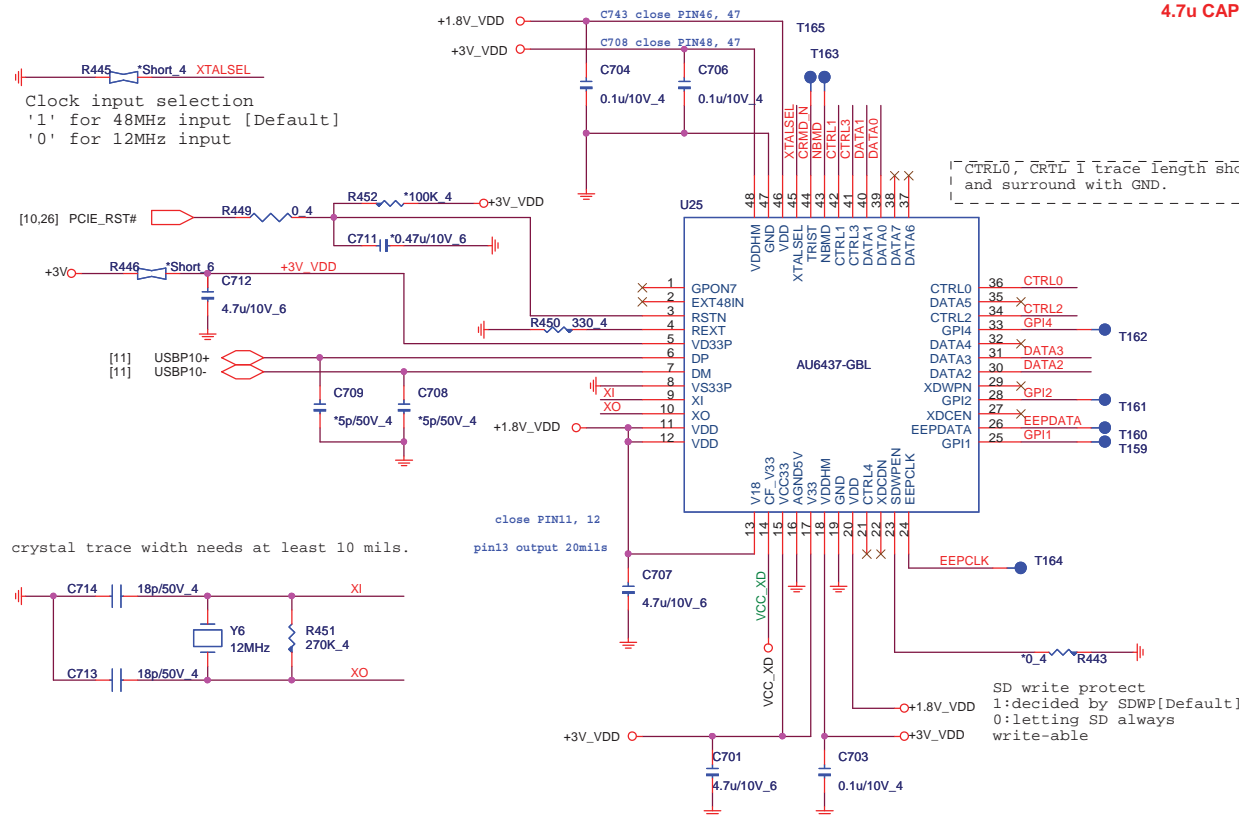
30

Main	DFHS11FR011
Second	DFHS11FR033

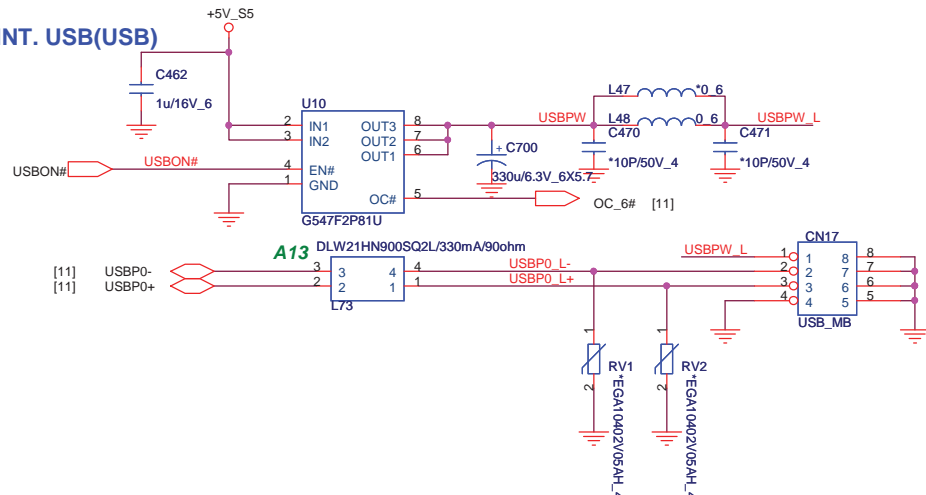


Close to CNxx pin 14 & pin23  
4.7u CAP close to pin23

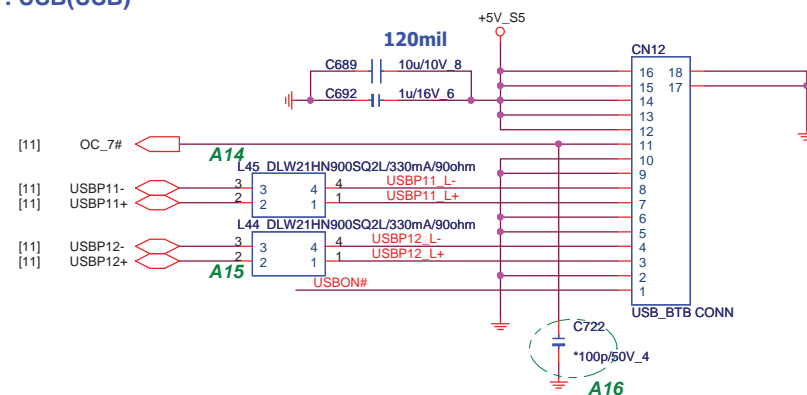
```
5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt
```



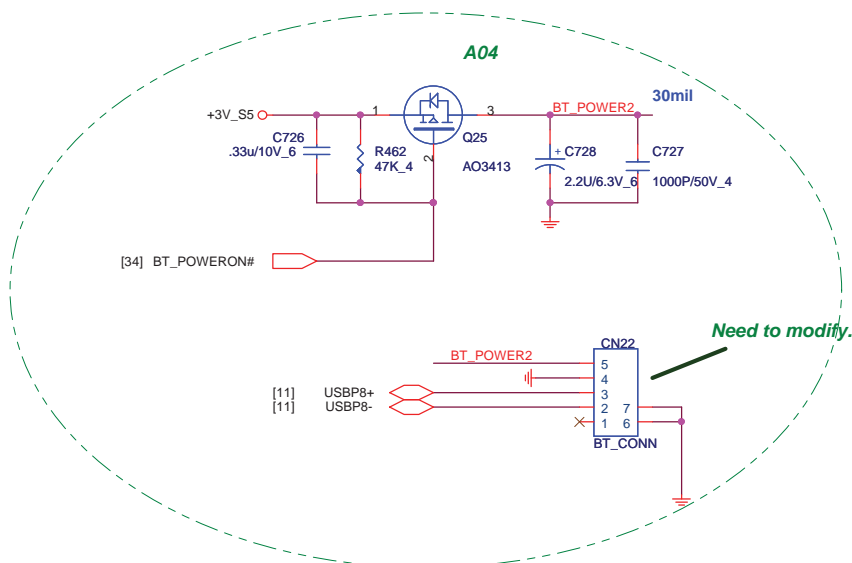
## INT. USB(USB)



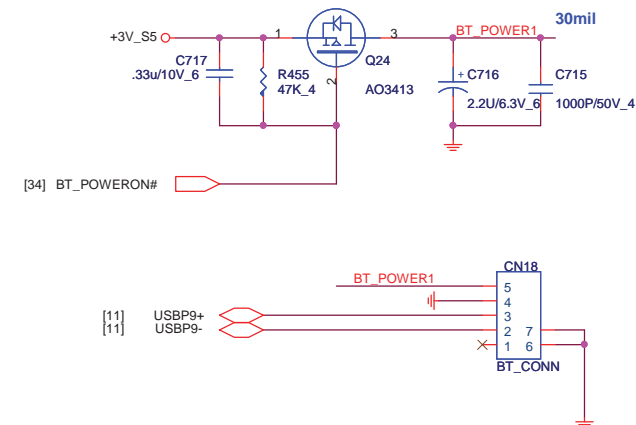
## EXT. USB(USB)



## BLUETOOTH V2.1 CONN(BTM)



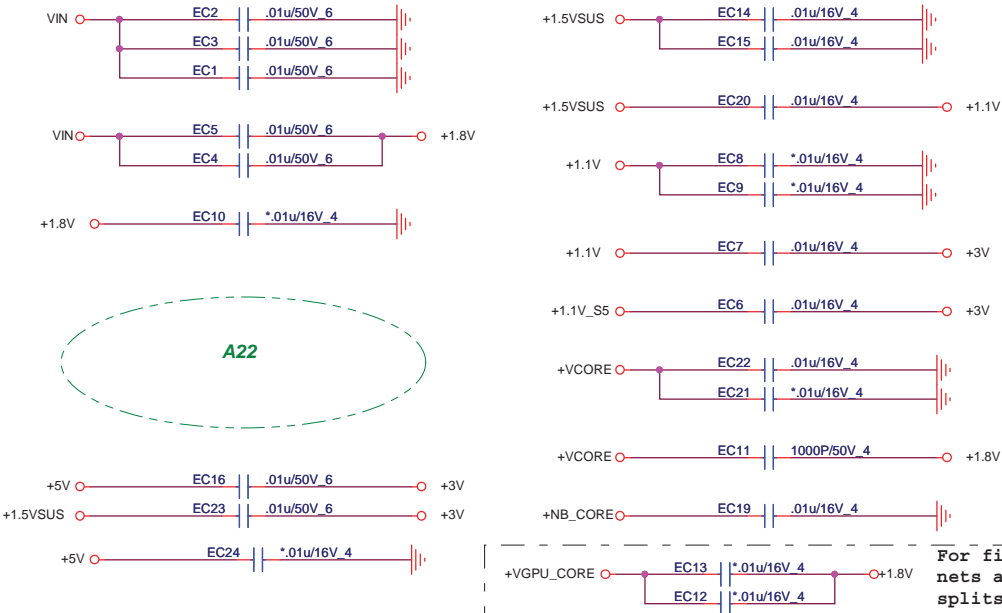
## BLUETOOTH V3.0 CONN(BTM)



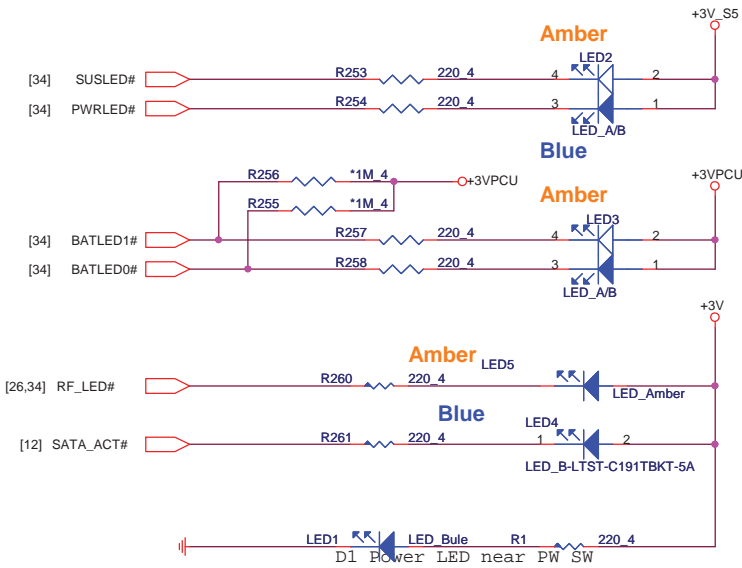
**PROJECT : ZQA**  
Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT/TP	1A
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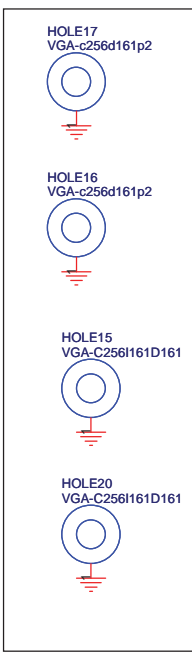
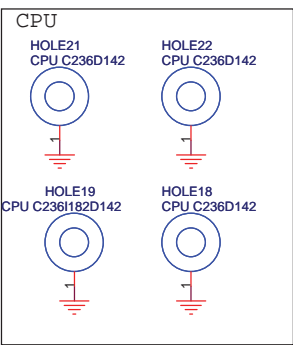
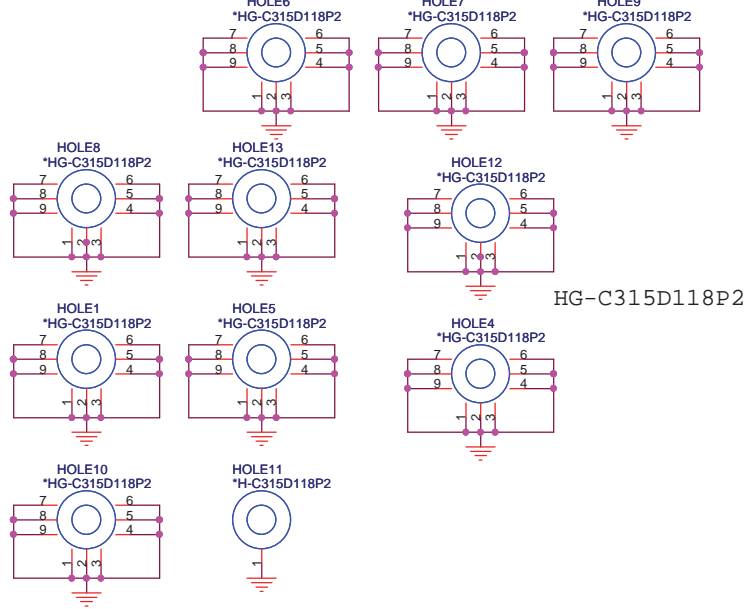
# EE RETURN-PATH CAPACITORS(EMC)




# LED(UIF)



# HOLE(OTH)

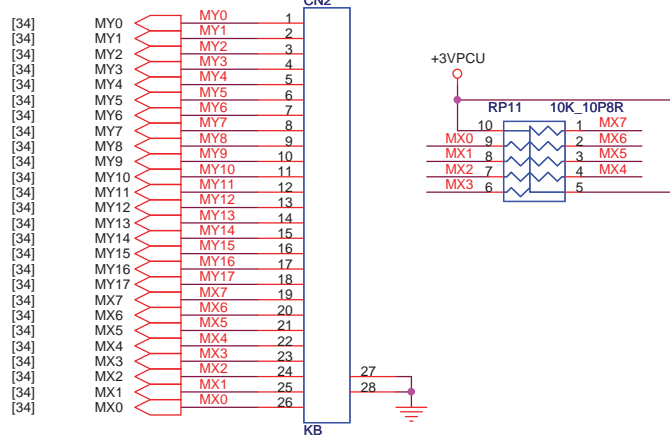




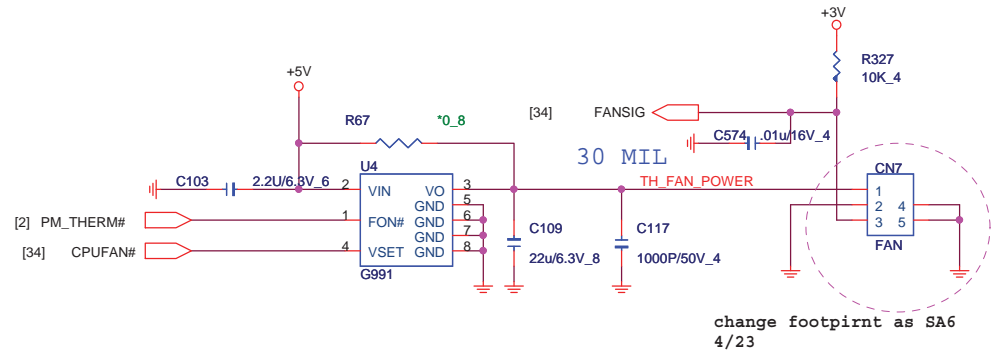
**PROJECT : ZQA**  
Quanta Computer Inc.

Size	Document Number <b>POWER/USB/BT/TP/MDC</b>	Rev 1A
Date: Monday, May 31, 2010	Sheet 32 of 48	

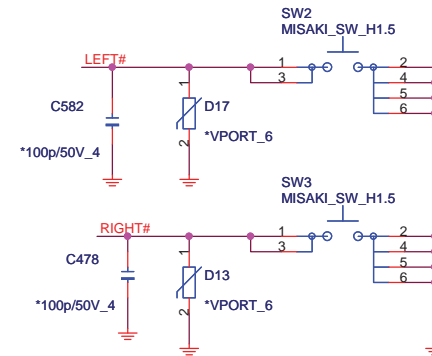
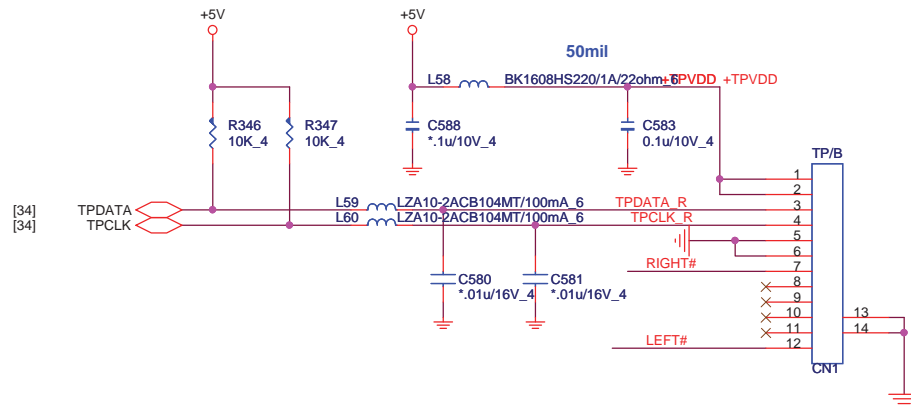
## K/B(KBC)



## CPU FAN(THM)



## TOUCHPAD BOARD CONN(TPD)

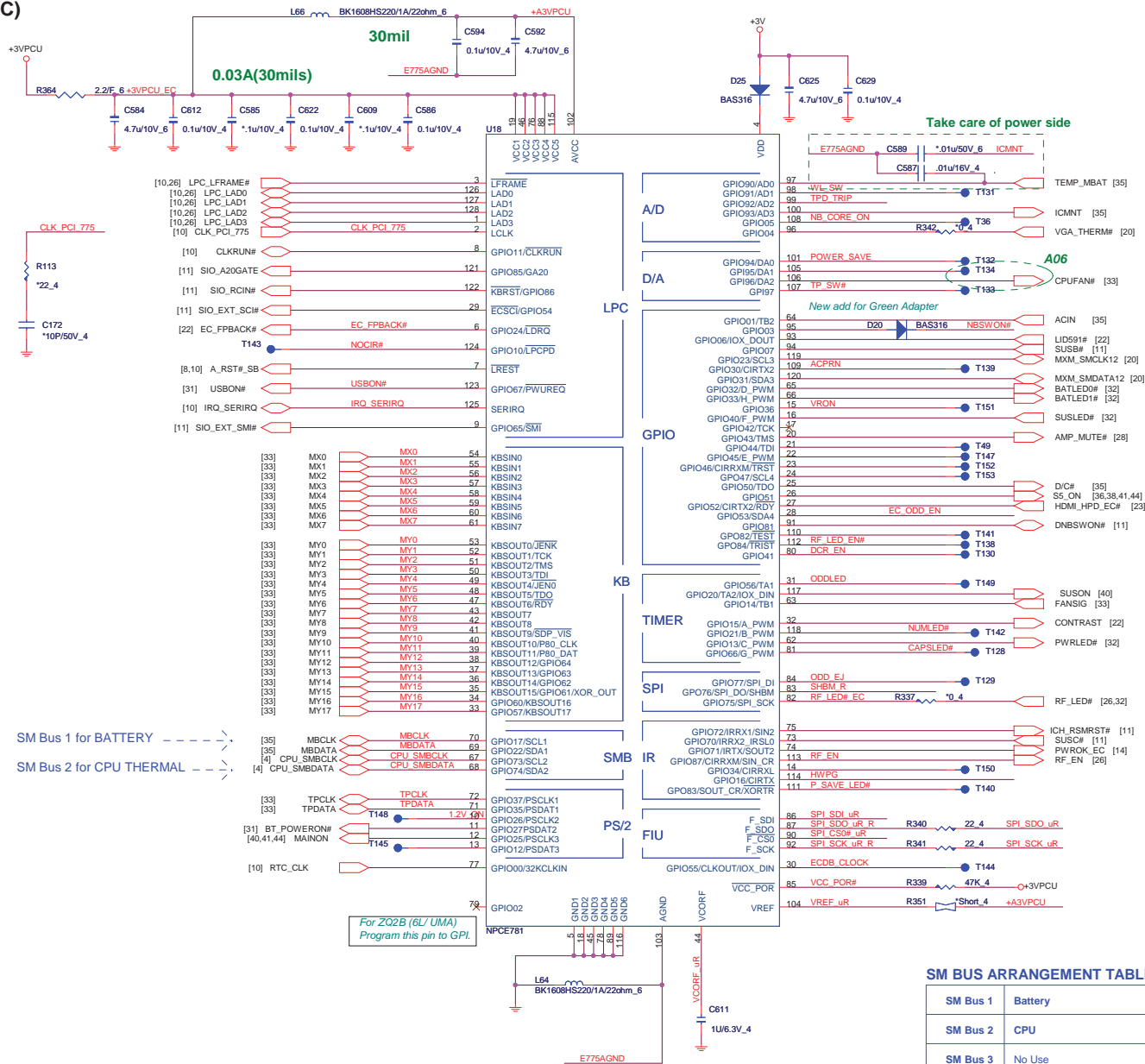


**PROJECT : ZQA**  
Quanta Computer Inc.

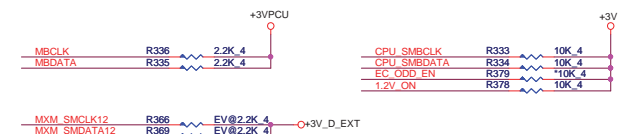
Size	Document Number	Rev
	<b>KB/FAN/EE RETURN CAP</b>	1A
Date:	Monday, May 31, 2010	Sheet 33 of 48



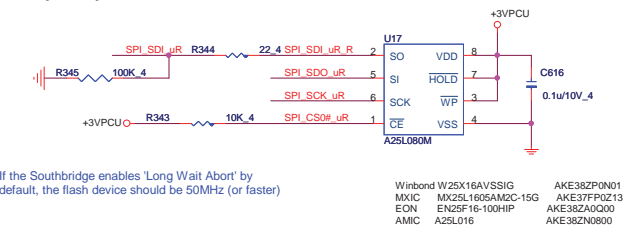
**EC(KBC)**



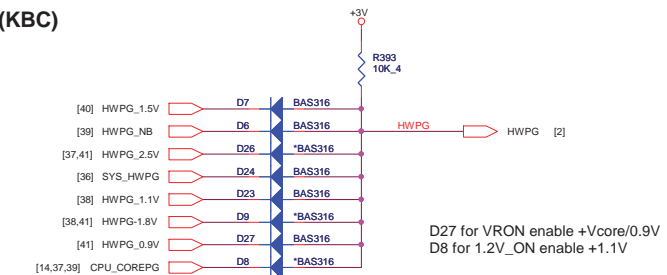
## SM BUS PU(KBC)



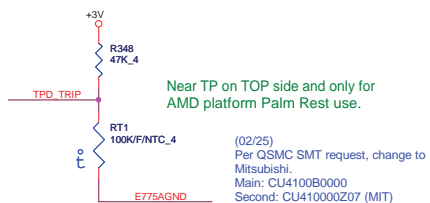
**SPI FLASH(KBC)**



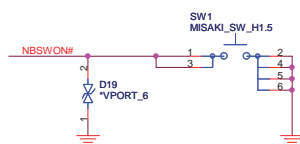
## HWPG(KBC)



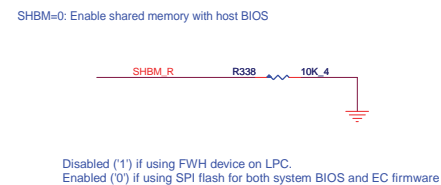
### PALM REST THERMAL SENSOR (THM)

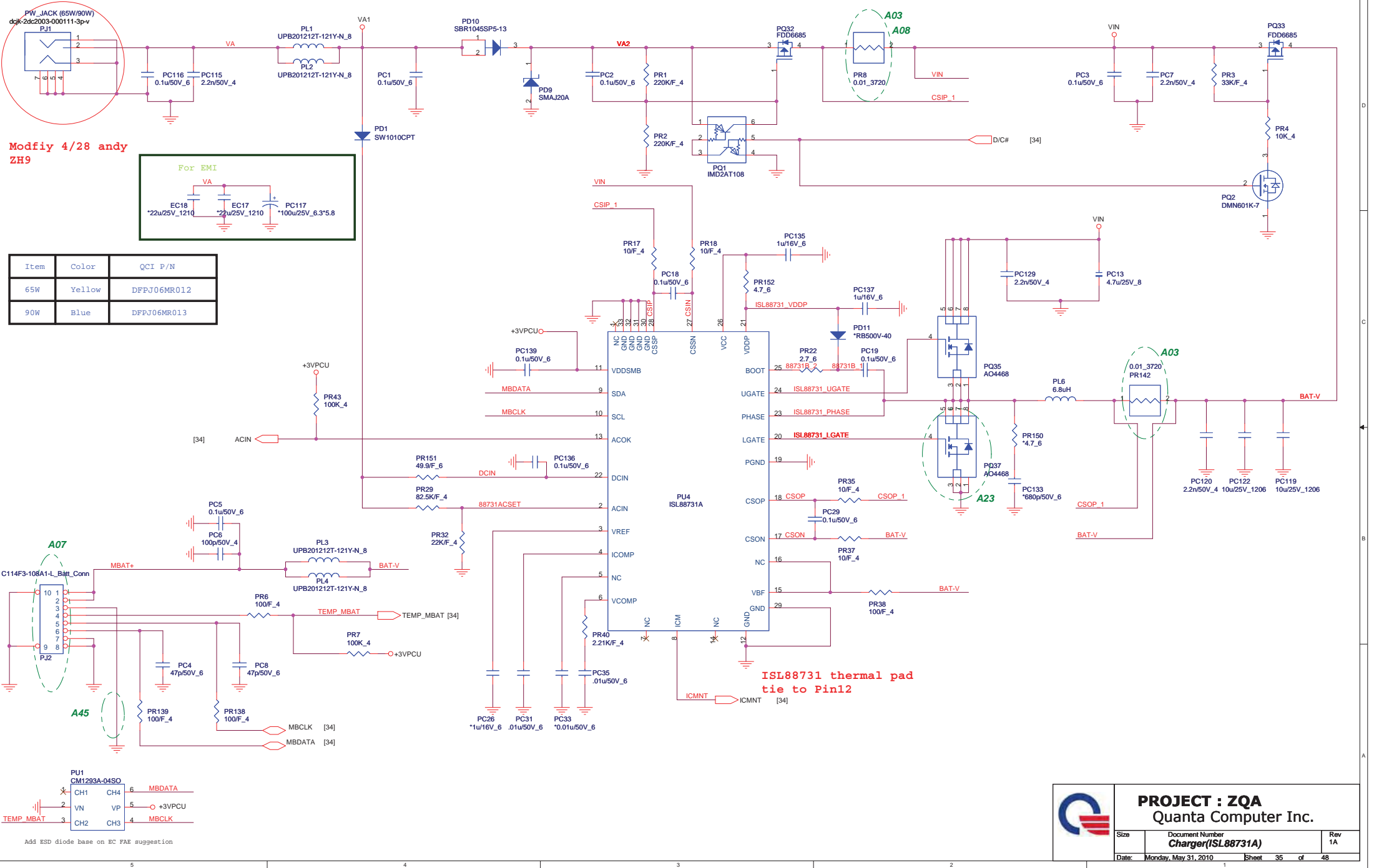


## POWER-ON SWITCH (KBC)



## POWER-ON SWITCH (KBC)






Modifiy 4/28 andy  
ZH9

Item	Color	QCI P/N
65W	Yellow	DFPJ06MR012
90W	Blue	DFPJ06MR013

A07

A45

ISL88731 thermal pad  
tie to Pin12



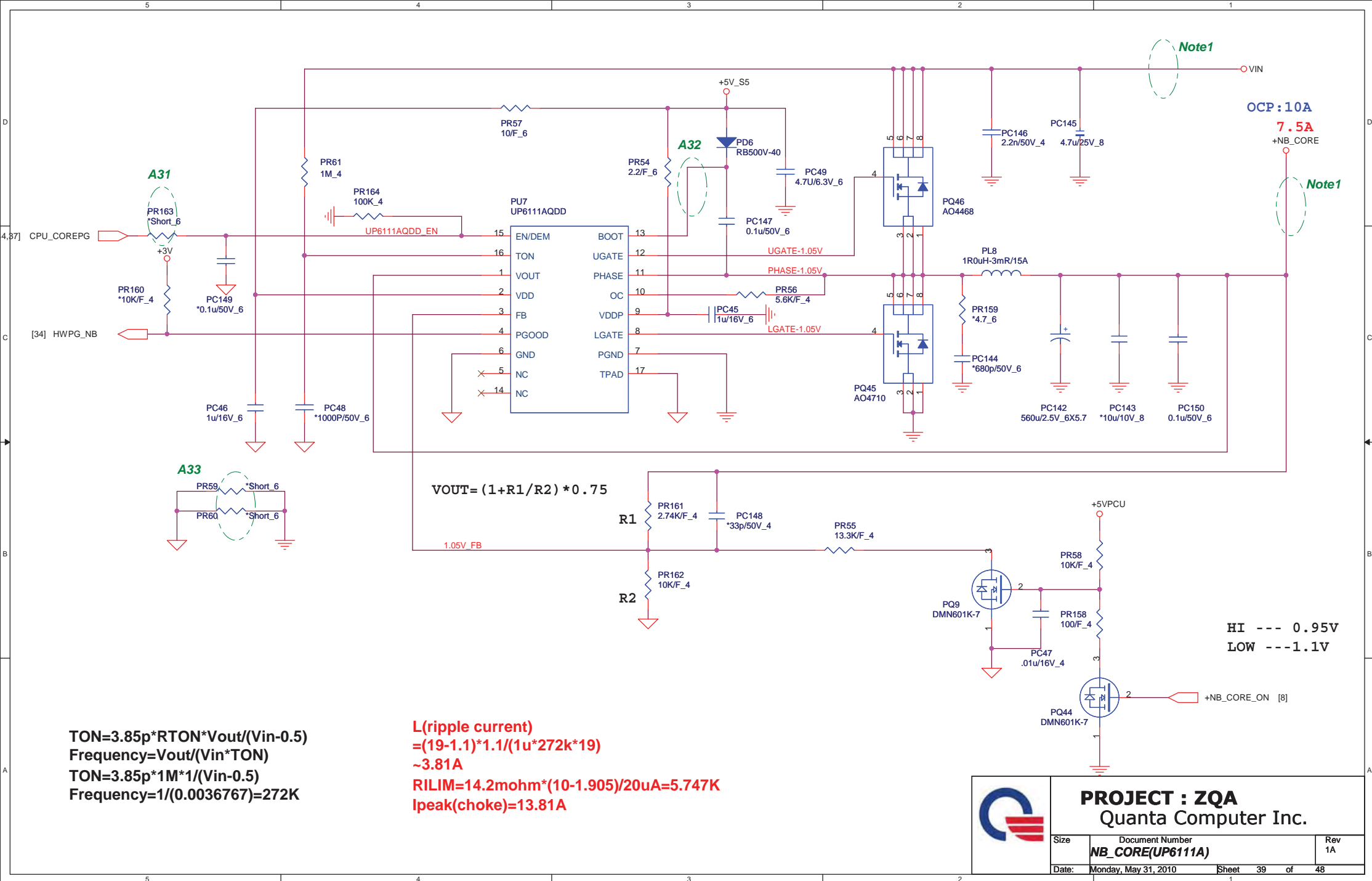
**PROJECT : ZQA**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>Charger(ISL88731A)</b>	1A
Date:	Monday, May 31, 2010	Sheet 35 of 48

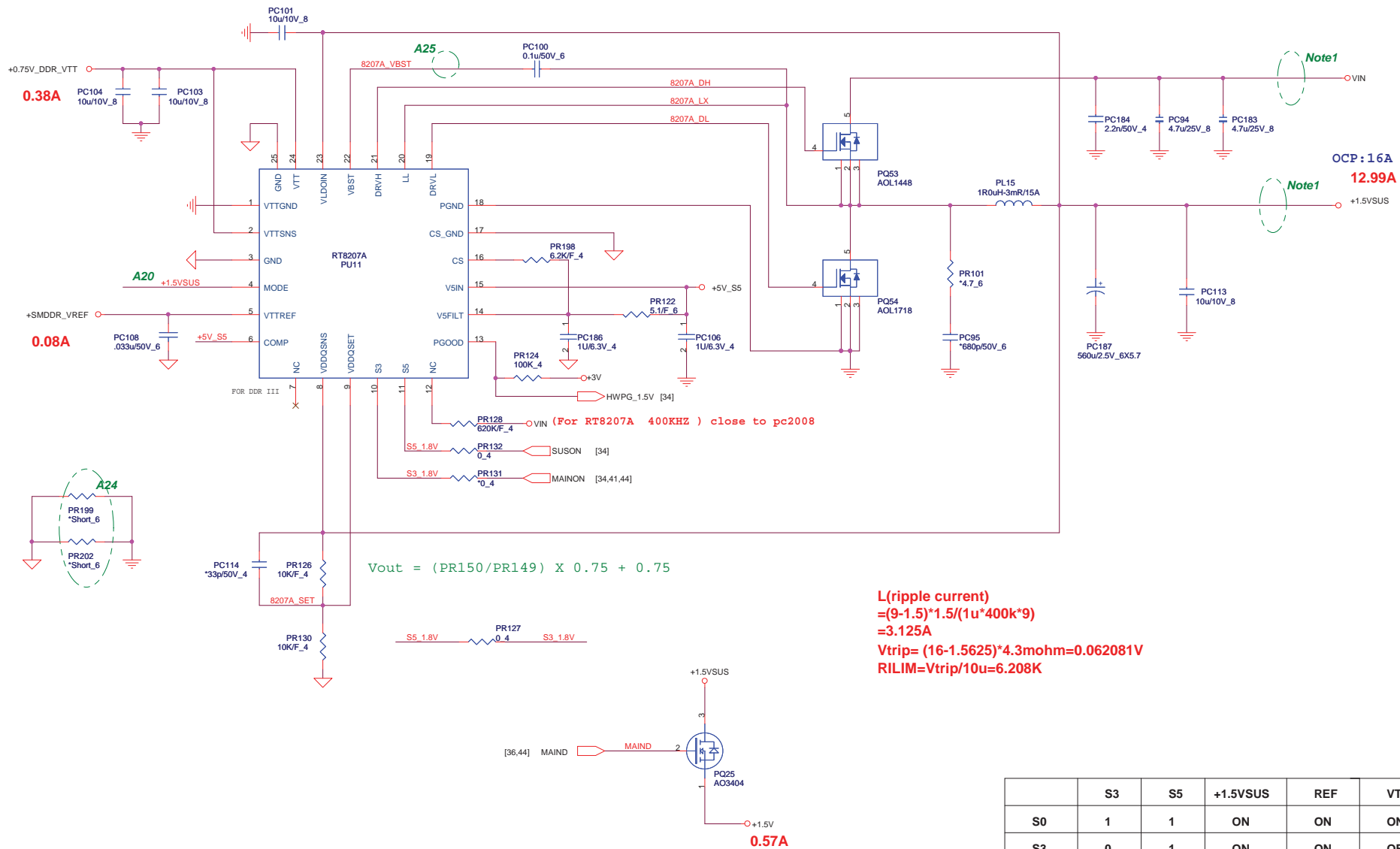










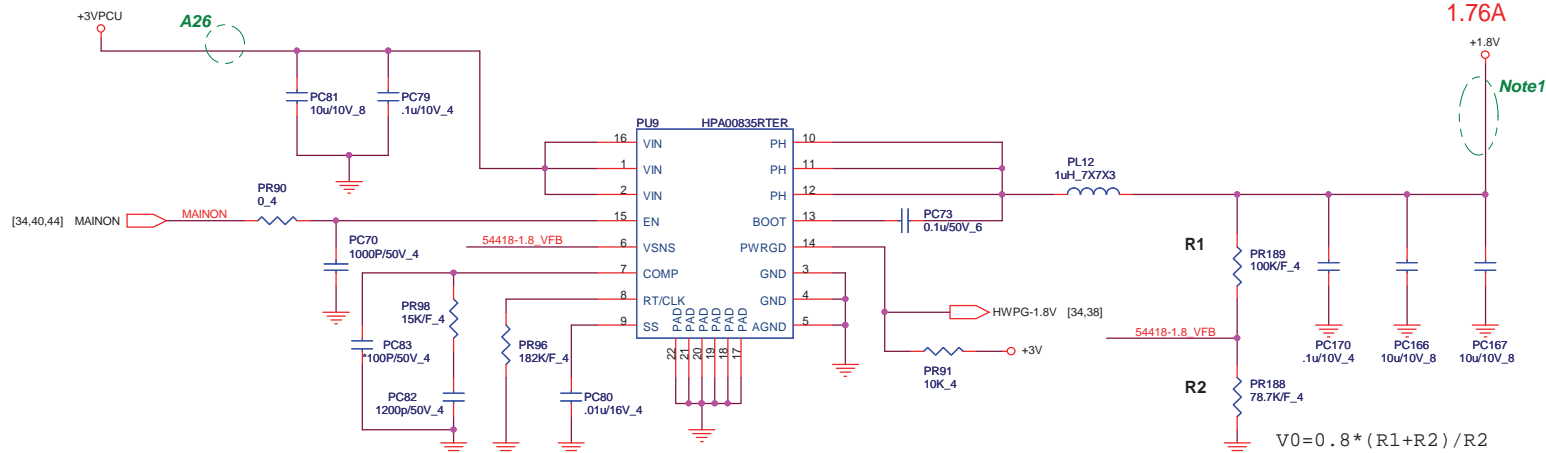
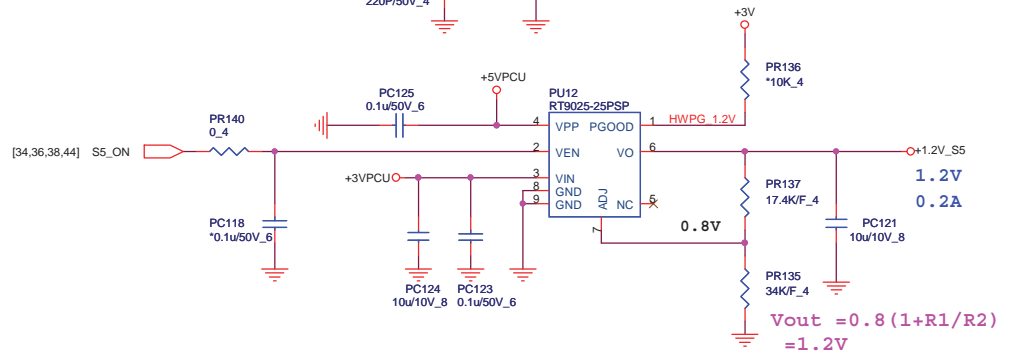
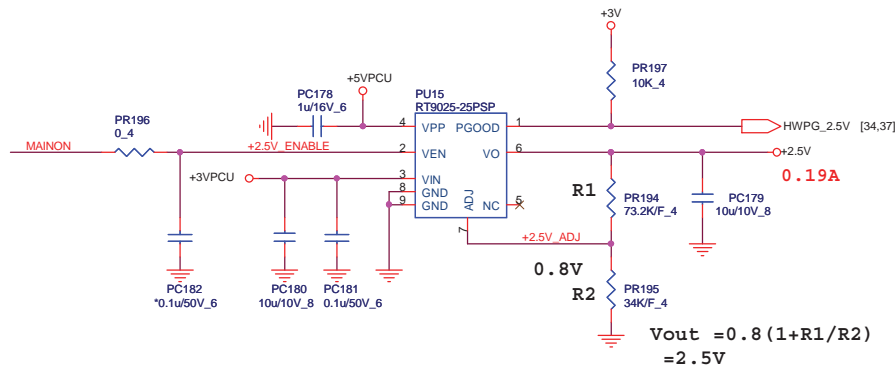
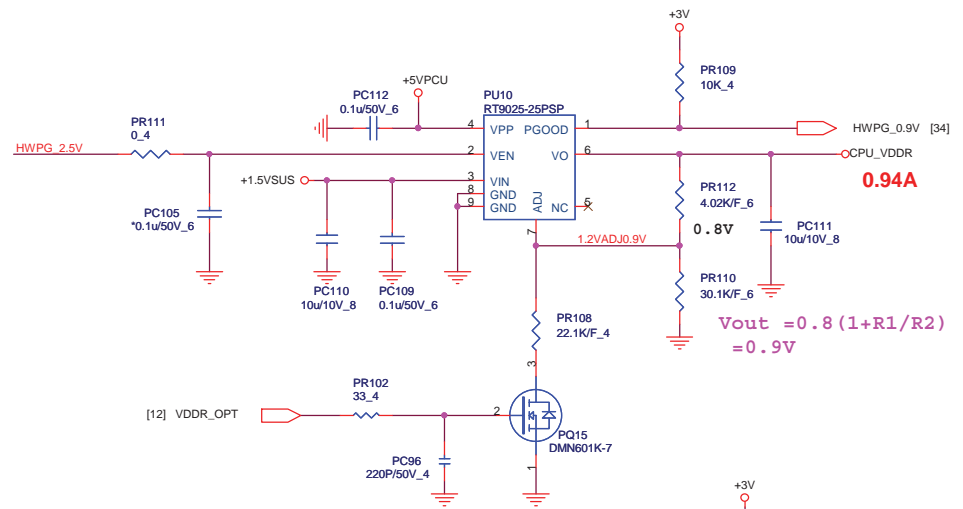
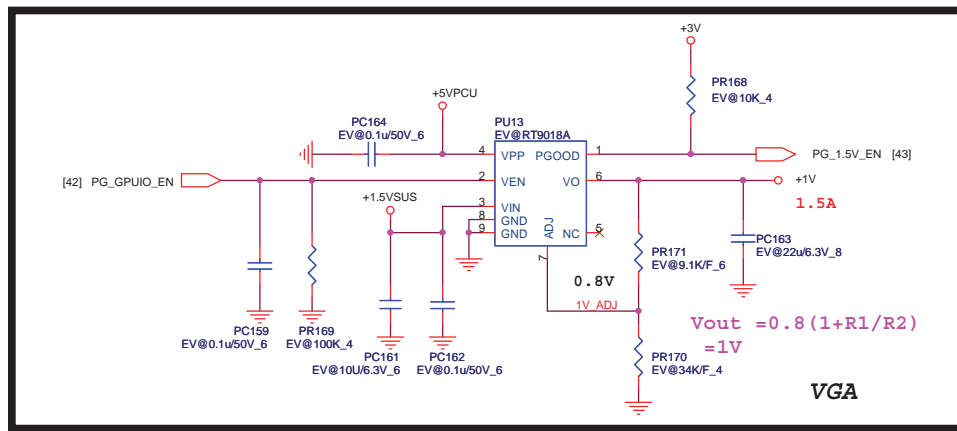


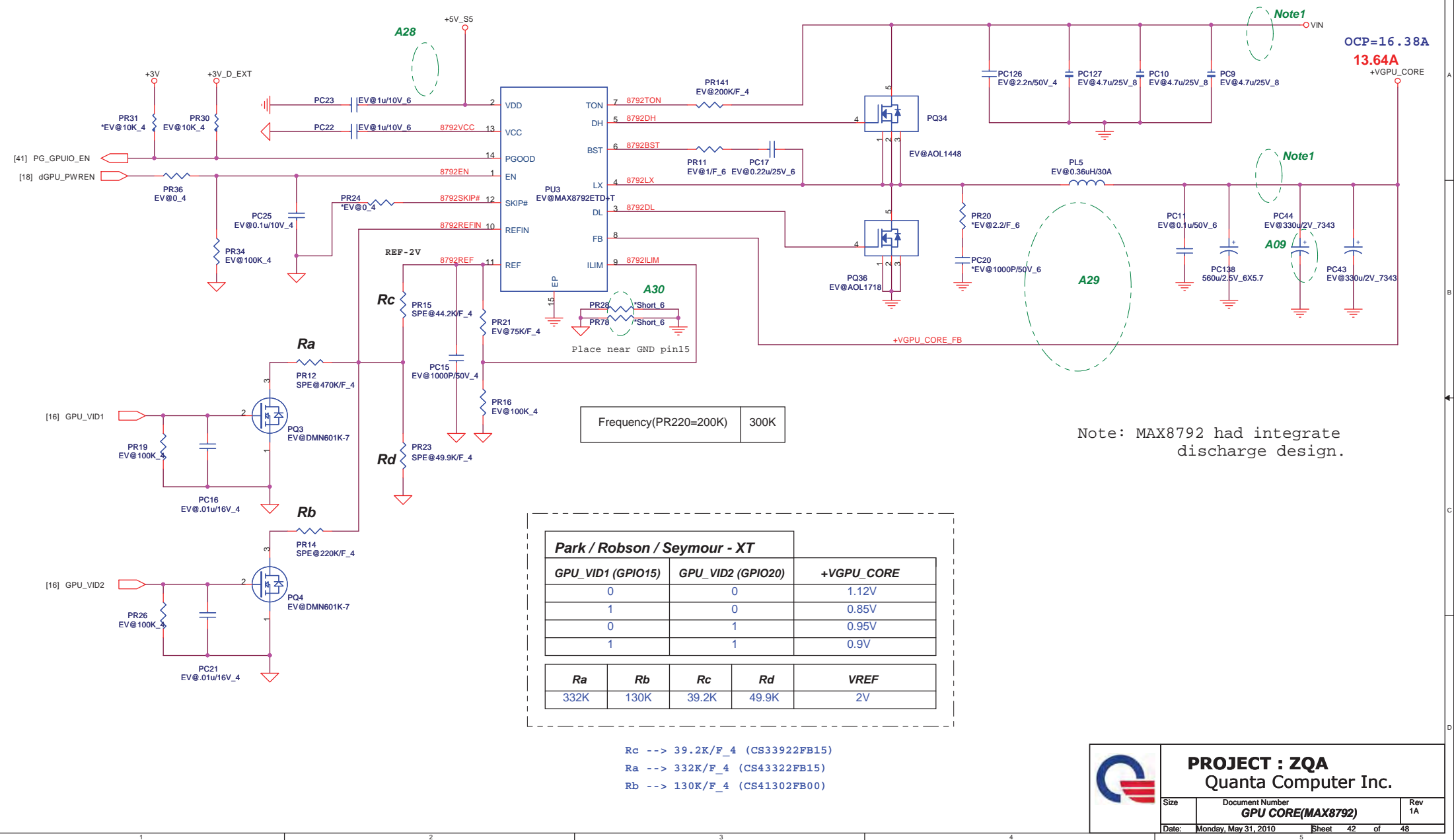
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF




**PROJECT : ZQA**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>DDR 1.5V(TPS51116)</b>	1A
Date:	Monday, May 31, 2010	Sheet 40 of 48

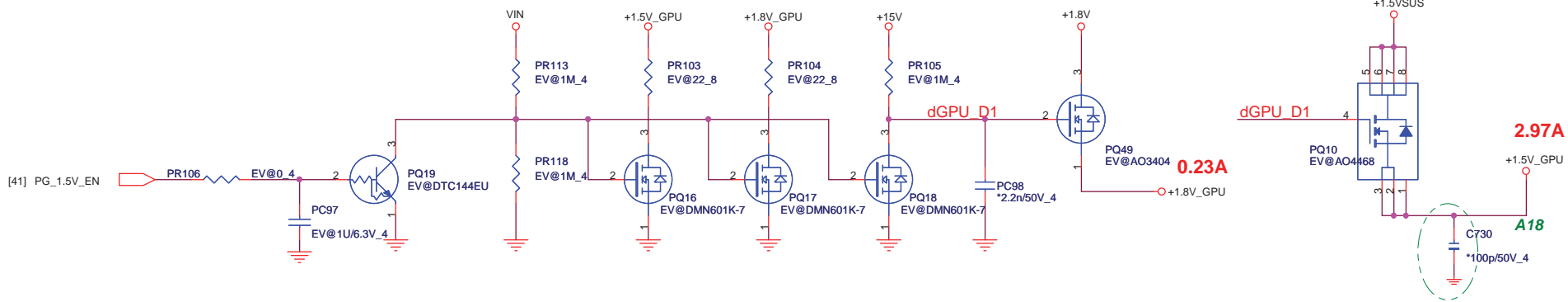






**PROJECT : ZQA**  
Quanta Computer Inc.

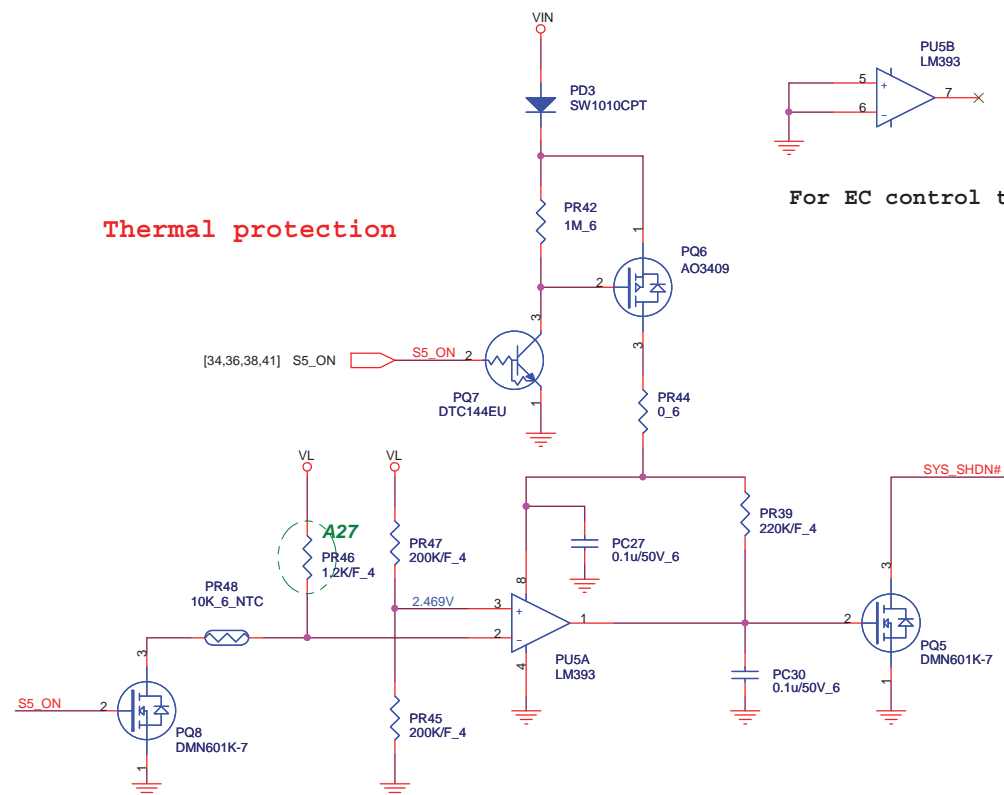
Size	Document Number <b>GPU CORE(MAX8792)</b>	Rev 1A
Date: Monday, May 31, 2010	Sheet 42 of 48	



**PROJECT : ZQA**  
Quanta Computer Inc.

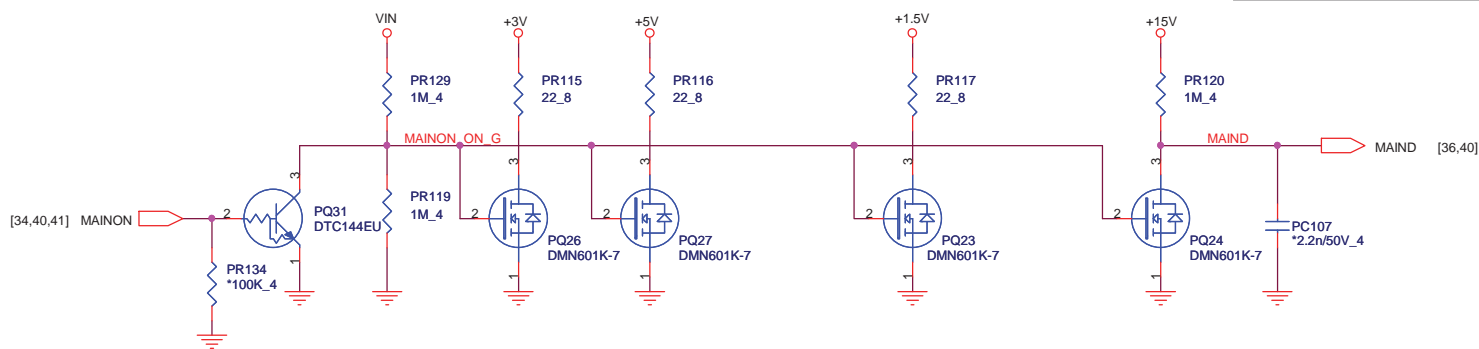
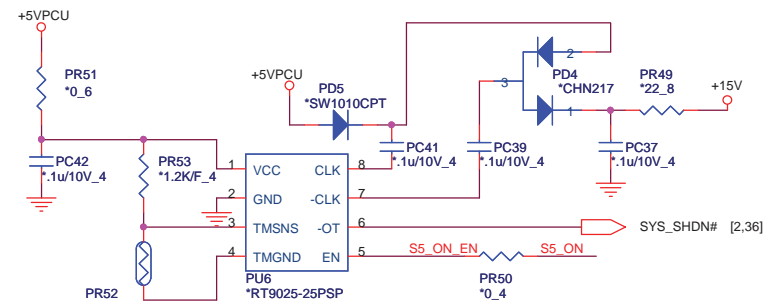
Size	Document Number <b>GPU POWER</b>	Rev 1A
Date: Monday, May 31, 2010	Sheet 43 of 48	

## Thermal protection



For EC control thermal protection (output 3.3V)

## POWER TEST : Thermal & Charge pump test circuit



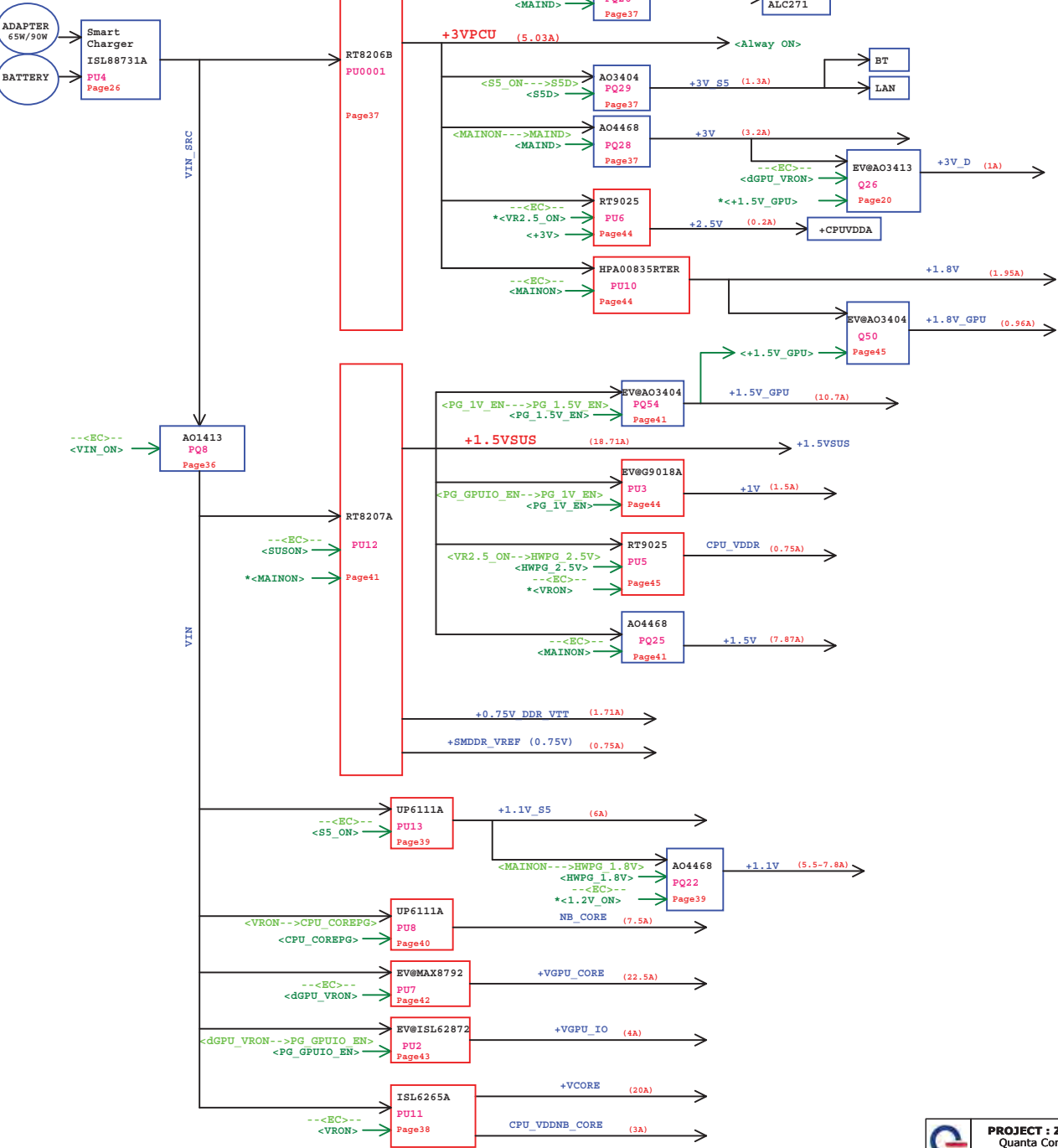
**PROJECT : ZQA**  
Quanta Computer Inc.



Size	Document Number	Rev
	<b>Thermal protect</b>	1A
Date:	Monday, May 31, 2010	Sheet 44 of 48

Size	Document Number <b>Power Sequence Chart</b>	Rev 1A
Date:	Monday, May 31, 2010	Sheet 45 of 48







MODEL	REV	CHANGE LIST	Model	KN1A M/B BOARD	
			Page	From	To
ZQA M/B	3A	<p>A01 PAGE28 : Add pull high resistor 4.7kohm on PD# pin, the reason is prevent speaker no sound.</p> <p>A02 PAGE28 : Change R229,R223 to 33K for speaker 1W.</p> <p>A03 PAGE35 : Change PR8,PR142 from 1m ohm to 10m ohm.</p> <p>A04 PAGE31 : Add BT2.1 design for Customer request.</p> <p>A05 PAGE22 : Delete R8 bead.</p> <p>A06 PAGE34 : The connection of CPUFAN# is changed from 105pin to 106pin.</p> <p>A07 PAGE35 : Change P/N</p> <p>A08 PAGE35 : Change PR8 Package to 3720</p> <p>A09 PAGE42 : Stuff PC44</p> <p>A10 PAGE37 : Stuff PC165</p> <p>A11 PAGE37 : Stuff PC153</p> <p>A12 PAGE36 : Change P/N</p> <p>A13 PAGE31 : Stuff L73</p> <p>A14 PAGE31 : Stuff L45</p> <p>A15 PAGE31 : Stuff L44</p> <p>A16 PAGE31 : Add 100p for EMI</p> <p>A17 PAGE23 : Add 1000p for EMI</p> <p>A18 PAGE23 : Add 1000p for EMI</p> <p>A19 PAGE02 : Delete R356</p> <p>A20</p> <p>A21</p> <p>A22 PAGE32 : Delete EC25,EC26,EC27,EC28</p> <p>A23</p> <p>A24</p> <p>A25</p> <p>A26</p> <p>A27 PAGE44 : Change PR46 from 1.7K ohm to 1.2K ohm.</p> <p>A28</p> <p>A29</p> <p>A30</p> <p>Note :</p> <p>1. Remove Jumper : JP5,JP16,JP6,JP14,JP3,JP13,JP11,JP2,JP8,JP9,JP10,JP15,JP17,JP12,JP1,JP7</p> <p>2. Remove 0 ohm :</p> <p>R355,R356,R370,183,R207,R73,R331,L61,R76,R65,R83,R42,R50,L9,R35,R24,R27,R448,R228,R204,R202,R199, R197,R195,R223,R424,R414,R400,R442,R459,R458,R446,R62,R70,R351.</p> <p>3. Change footprint :</p> <p>C119,C139,C149,C153,C154,C181,C182,C185,C191,C192,C195,C198,C199,C201,C202,C204,C205,C209, C217,C218,C222,C224,C225,C233,C234,C235,C236,C242,C248,C249,C252,C255,C260,C261,C262,C263, C266,C268,C270,C273,C275,C277,C280,C285,C304,C307,C313,C314,C316,C318,C328,C329,C330,C332, C335,C336,C337,C338,C340,C361,C362,C363,C364,L30,L39,R9,R84,R89,R95,R96,R98,R123,R126,R134, R158,R363,C296,C308,C213</p>	1	1A	3A
			2	1A	3A
			3	1A	3A
			4	1A	3A
			5	1A	3A
			6	1A	3A
			7	1A	3A
			8	1A	3A
			9	1A	3A
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			12	1A	3A
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			48	1A	3A
			<div><div></div><div>PROJECT : ZQA Quanta Computer Inc.</div></div> <div><div>Size Custom</div><div>Document Number</div><div>Rev 3A</div></div> <div>CHANGE LIST - 3A</div> <div><div>Date: Monday, June 21, 2010</div><div>Sheet 48 of 48</div></div>		
<div> Quanta Computer Inc. ZQA</div>		PROJECT: ZQA	PCBA NO.	REV: 3A	DOC. NO :
APPROVED BY : Johnny O		CHECK BY : Darren Liao	DRAWING BY : Bowen Chuang	DATE :06/11/2010	SHEET 1